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MAR 18

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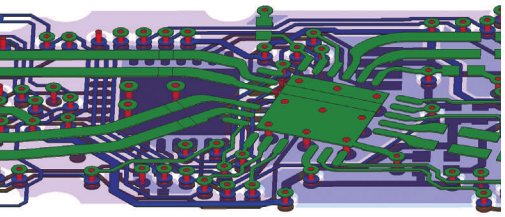

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by Paul Rako, Technical Editor

Polyphase filters reduce saturation

by Ron Warner, Lattice Semiconductor Corp

Active heat removal cools electronics hot spots

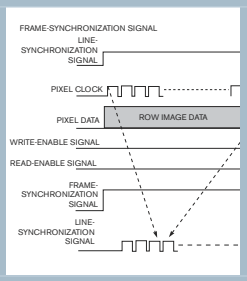
by Paul Magill, PhD, Nextreme Thermal Solutions Inc

Integrating midsized LCDs

 by Calvin Du, MedX Health Corp

pulse

DESIGNIDEAS



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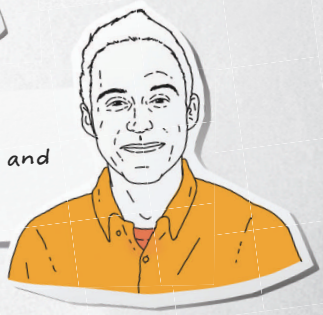

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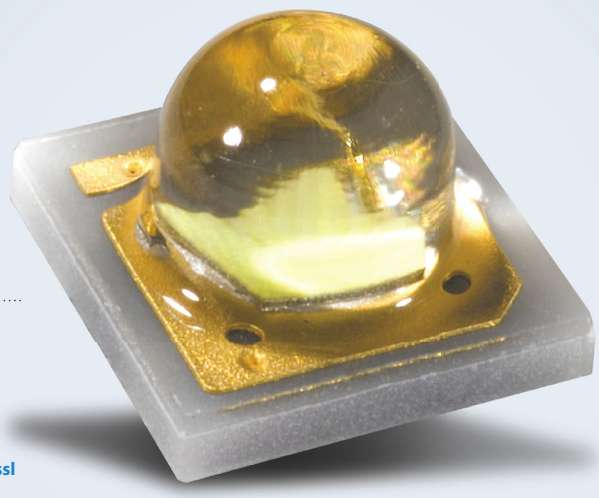

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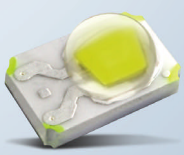

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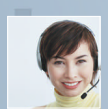

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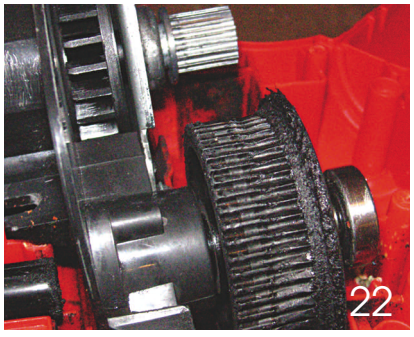
SPECIAL SECTION

Scrutinizing LED lighting

51 The LED-technology sector continues to be a growing industry. But its complex design requires integration of several potentially problematic components.

by Margery Conner, Technical Editor



DEPARTMENTS & COLUMNS

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Combating congestion in high-performance, low-cost systems on chip
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Microsoft puts a bullet in my laptop
from Leibson's Law, by Steve Leibson
I'm not a knowing pirate; in fact, I consider myself a victim. But Microsoft was able to reach into my PC and brand me a pirate nevertheless. My mistake. I pay the price.
➔www.edn.com/100318toc1

Google's Nexus One: initial hands-on frustrations and fun
from Brian's Brain, by Brian Dipert
I swapped my friend's SIM card out of her T-Mobile G1 and into the Nexus One, and since then we've both been evaluating the old-versus-new hardware and software.
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BY RON WILSON, EXECUTIVE EDITOR

What happens after "I'm sorry": the world of product engineering

Senior chip designers generally have a good understanding of the whole design flow. Fewer, even among senior designers, can speak with confidence about the tasks that start when silicon appears—the silicon bring-up process. And fewer still can speak comfortably about what happens when the new chip fails to come up properly: the realm we used to call failure analysis. That lack of information needs to change, argue two executives of that world, Presto Engineering's chief executive officer, Michel Villemain, and vice president of engineering, Frank Sauk.

To begin with, the two would like to change the name from failure analysis to product engineering. The reasons are deeper than just marketing spin. Villemain explains that there has been a profound shift in recent years in what actually goes on at this stage in the life of an IC design.

"A few years ago, a failure-analysis lab would have a focused-ion-beam system and maybe two or three additional pieces of equipment," he relates. When your chip didn't work, you'd record its faulty behavior on the bring-up bench, diagnose the problem, develop a proposed ECO (engineering change order) in simulation, and then send a die to the failure-analysis lab. The turnaround would be about 24 hours, and you could spin a mask with confidence.

Since then, SOCs (systems on chips) have gone from four metal layers to 18. Access through the top of the die is impossible. So analysis of the die begins with lapping the back until the silicon is so thin that it's transparent and then retesting to make sure that you haven't broken anything. Probing and measuring then require a battery of mad-scientist tools, such as IR (infrared) imagers, lasers, and optical probes. "We are dealing with not-well-understood proxies of the signals we would really like to measure," Villemain says. Further, SOCs are so dependent on software to place them in a particular mode or state that the chip often must connect to system stubs and run real software just to establish the diagnostic loops that will create patterns for the probing equipment.

Product engineering needs a new relationship with design and with the EDA industry.

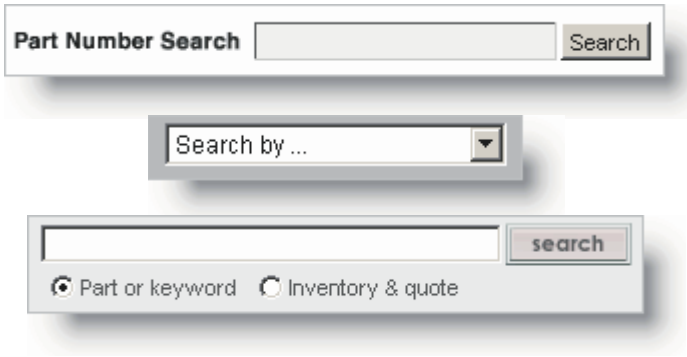
The nature of the questions has changed, as well, Villemain continues. In the 180-nm days, the questions tended to be straightforward: Where is this signal getting inverted? Why isn't the bus request reaching the output pin? Today, the questions may leave product engineers with a lot less to go on. Where is all that leakage current coming from? Why isn't anything coming out of this scan chain? And turnaround times have stretched from hours to weeks. These changes justify the name change.

The changing environment requires more than new words, however. Product engineering needs a new relationship with design and with the EDA industry, Villemain and Sauk insist. "Designers need a primer—something to tell them this is what happens after tapeout," says Villemain.

Sauk agrees. "Design engineers need to understand what is and isn't possible in the lab and plan for product engineering as part of the process, not as some worrisome last resort," he says. That would mean, for instance, understanding the access requirements of the backside probing tools, and being prepared to help product engineers navigate the design database. Even such steps as preparing the die for the correct tool before sending it to the lab can make a week's difference in turnaround, Villemain says. Further, design teams could adjust their physical-design styles to assist the new tools, just as today backend designers place spare gates and ease congestion near suspicious circuits just in case there's a metal-mask ECO.

Similarly, product engineering needs a closer relationship with the EDA industry. "The test industry has DFT [design for test]," Villemain says. "We need to push for the EDA companies to understand that they have a significant role in product engineering, as well."EDN

Contact me at ronald.wilson@reedbusiness.com.



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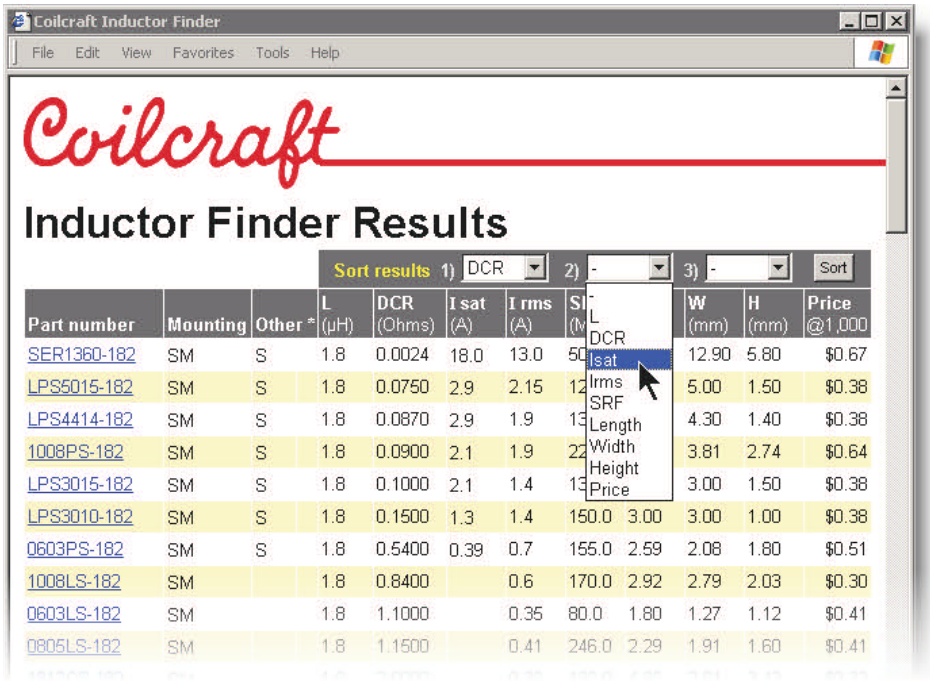

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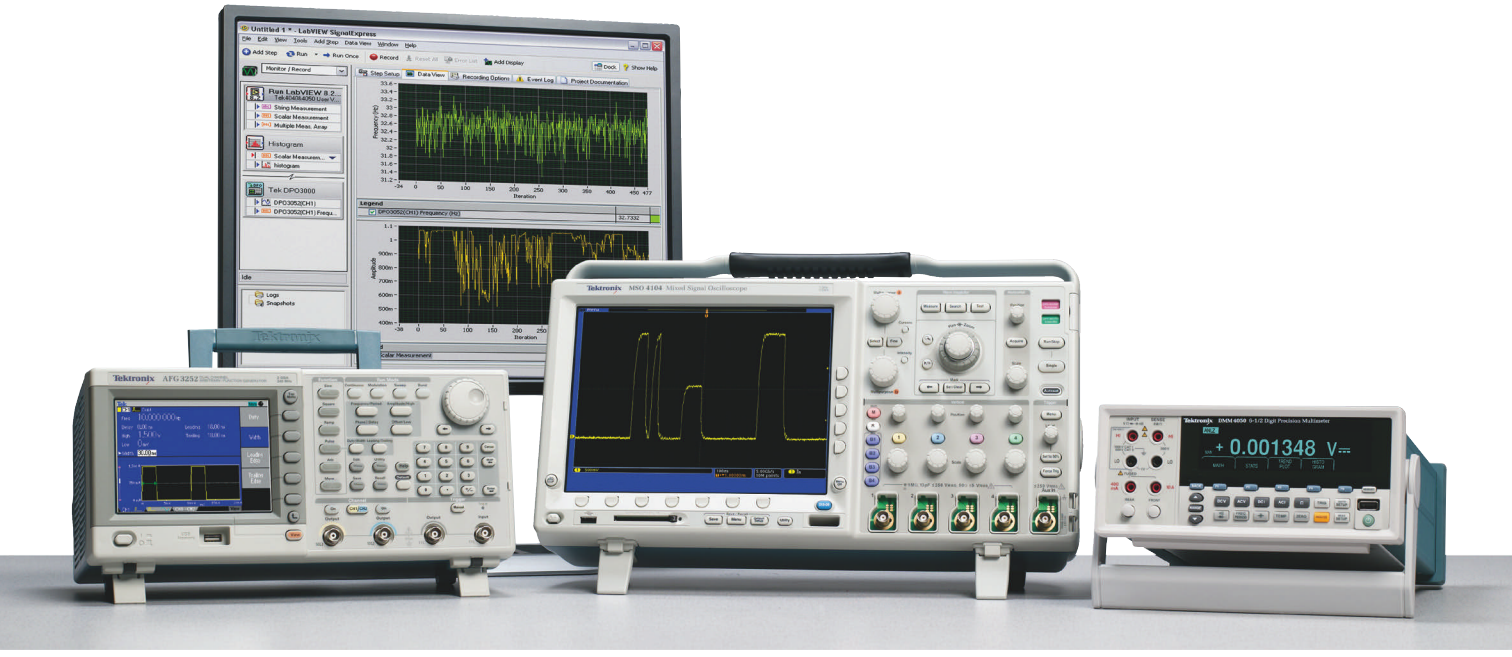

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pulse

INNOVATIONS & INNOVATORS

Broadband VNA systems accurately characterize RF devices' nonlinear behavior

Anritsu has introduced a nonlinear-measurement system comprising its VectorStar broadband VNA (vector-network-analyzer) hardware and software that addresses the market demand for precise nonlinear vector analysis. The system enables engineers to accurately characterize the nonlinear behavior of RF devices, such as power amplifiers for emerging wireless-communication designs. The system offers a variety of configurations, provides fast measurements through real-time tuning, and performs accurate load-pull measurements, eliminating hours of load-pull-tuner calibration time. In addition, the system works with customer-owned tuners, permitting low-cost upgrades and allowing incremental configuration for true balanced-differential active-device measurements.

The unit achieves the industry's best performance by integrating the VectorStar hardware with software that uses a new approach to acquiring the data necessary for nonlinear-device design and optimization. The software, which Anritsu developed with HFE SAGL (High-Frequency Engineering Società a Garanzia Limitata, www.hfemicro.com), provides nonlinear information in a variety of formats to facilitate RF-device analysis, design, and evaluation. By supporting the use of passive or active tuners or a combination of both, the hardware provides the most complete and accurate nonlinear load-pull data and offers the lowest-cost upgrade paths. The system inserts a low-loss coupler between the DUT (device under test) and the tuner to achieve accurate DUT source- and load-impedance measurements. The software provides immediate display of the DUT's performance based on changes in impedance, allowing for real-time tuning. This approach also eliminates the need for precalibrated tuners and, by allowing monitoring of the DUT impedance during measurements, reduces the importance of tuner repeatability.

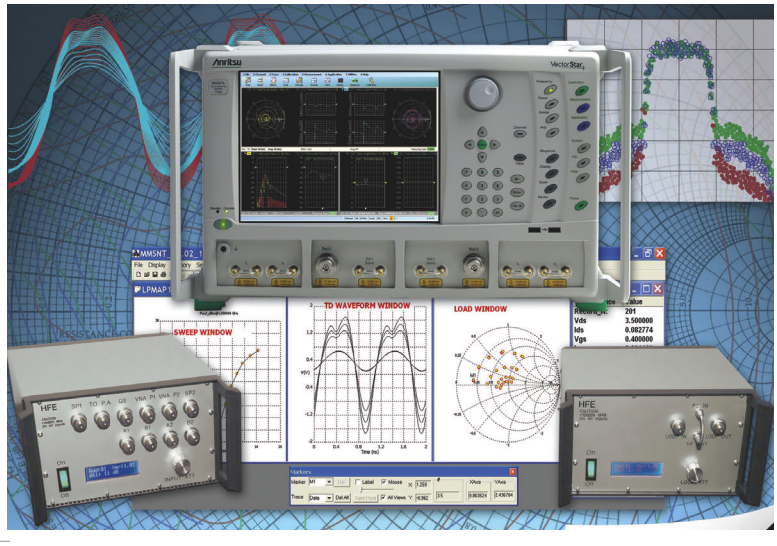
The unit can also provide a nonlinear DUT's measured parameters. You can use these parameters to design an optimum impedance-matching network, or, for model simulation and development, you can export the parameters to an EDA program, such as Microwave Office (http://web.awrcorp.com/Usa/Products/Microwave-Office). Anritsu officials believe that the choice of immediate design or model simulation is superior to the black-box-only approach of systems that require an EDA program. The US price starts at $231,875 for the 20-GHz nonlinear system. Current VectorStar VNA users can easily upgrade to a nonlinear system by adding the software, test set, and components.**—by Dan Strassberg**

▷**Anritsu**, www.anritsu.com.

FEEDBACK LOOP

"Don't people realize how dangerous tampering with our brains is? ... Nobody touches my brain, and nobody decides where I look but me!"

—Controls engineer Bruce Koerner, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6718485. Add your comments.



Based on the manufacturer's VectorStar broadband VNA, this system measures nonlinear RF-device parameters with what the company terms unsurpassed accuracy.

PLX delivers differentiation through evolution

PLX Technology recently announced its third generation of NAS (network-attached-storage) devices and the first it developed under the PLX umbrella (see "Integration amassed: analyzing a NAS," *EDN*, Jan 21, 2010, pg 16, www.edn.com/article/CA6715773).

The NAS 7820, 7821, and 7825 embed dual ARM 11 microprocessor cores running at 750 MHz, a companion network processor, and various application-specific hardware engines and software-acceleration modules. Single- and dual-port RGMII (reduced-gigabit-media-independent-interface) support enables integrated router and gateway functions, and two of the three family members embed dual SATA (serial-advanced-technology-attachment) transceivers for RAID (redundant-array-of-inexpensive-disk) capabilities.

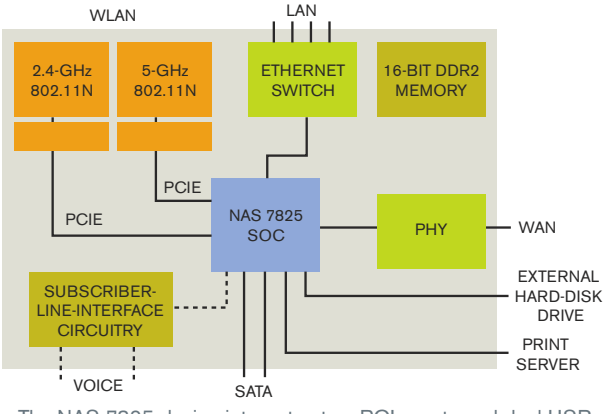
Other differentiators include two PCIe (Peripheral Component Interconnect Express) Version 1.0 ports on the high-end 7825 and one each on the other two products, along with dual USB (Universal Serial Bus) 2.0 transceivers on all three devices. They all offer UART (universal-asynchronous-receiver/transmitter), SPI (serial-peripheral-interface), I²C (inter-integrated-circuit), and JTAG (Joint Test Action Group) capabilities, and the 7825 also has SPDIF (Sony/Philips digital-interface-format) and TDM (time-division-multiplexed)/PCM (pulse-code-modulation)-interface features, targeting applications such as digital video recorders and set-top boxes.

> PLX's processors can directly boot from the system's disk drives.

The devices' GbE (gigabit-Ethernet) MAC (media-access controller) includes a bandwidth-boosting TCP/IP (Transmission Control Protocol/Internet Protocol) offload engine. Integrated SRAM holds frequently used data, and onboard nonvolatile semiconductor storage is unnecessary because PLX's processors can directly boot from the system's disk drives. The devices and their companion development kits will enter general sampling this quarter; full production will follow in the second quarter. The NAS 7825 costs $15 (volume quantities), and the 7821 and 7820 sell for $13 and $11, respectively. All three devices come in a 17×17-mm, 256-bump FBGA package.

—by Brian Dipert

▷**PLX Technology**, www.plxtech.com.



The NAS 7825 device integrates two PCIe ports and dual USB 2.0 transceivers.

DILBERT By Scott Adams

BAR CODE ENABLES TRACEABILITY FOR INDIVIDUAL LEDs

03.18.10

Some automotive and consumer-electronics customers require traceability down to the component level, and, for that reason, Philips Lumileds has implemented complete forward and backward traceability for its Luxeon power-LED product line. This feature allows the company to identify hundreds of

Bar codes allow full traceability for Luxeon power LEDs.

millions of LEDs' time, location, and technology of manufacture–down to the wafer level. The company claims that it is the first LED manufacturer to adopt this level of manufacturing control. Philips expects the solid-state lighting industry to require a similar degree of traceability.

—by Margery Conner

▶**Philips Lumileds, www.philipslumileds.com.**

One-step graphene doping could enable graphene CMOS transistors

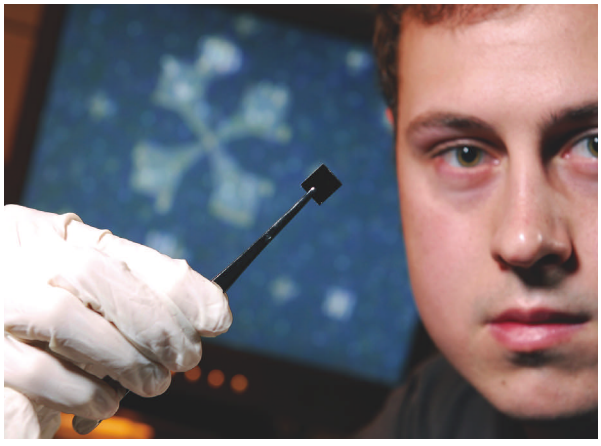
Researchers at the Georgia Institute of Technology have claimed a one-step process that produces both N- and P-type doping of large-area graphene surfaces and that could facilitate the use of the material for future electronic devices. The doping technique, which the researchers produced by applying a commercially available SOG (spin-on-glass) material to graphene and then exposing it to electron-beam radiation, can also increase conductivity in graphene nanoribbons for interconnects.

The team created both types of doping by varying the exposure time to the e-beam radiation; higher levels of e-beam energy produce P-type areas, and lower levels produce N-type areas. The researchers used the technique to fabricate high-resolution PN junctions. When the team properly passivates the SOG, it creates doping that should remain indefinitely in the graphene sheets.

"This is a step toward making possible complementary-metal-oxide graphene transistors," says Raghunath Murali, a senior research engineer in Georgia Tech's Nanotechnology Research Center.

In the doping process, Murali and graduate student Kevin Brenner removed flakes of one- to four-layer-thick graphene from a block of graphite. Next, they placed the material onto a surface of oxidized silicon and fabricated a four-point contact device. They then spun on films of HSQ (hydrogen silsesquoxane) and cured certain portions of the resulting thin film using e-beam radiation. The technique provides precise control over the amount of radiation and where it is applied to the graphene; higher levels of energy correspond to more cross-linking of the HSQ.

"We gave varying doses of electron-beam radiation and then studied how it influenced the properties of carriers in the graphene lattice," says Murali. "The e-beam gave us a fine range of control that could be valuable for fabricating nanoscale devices. We can use an electron beam with a diameter of 4 or 5 nm that allows very precise doping patterns." Electronic measurements show that the technique creates a graphene PN junction with large energy separations, indicating strong doping effects.



Georgia Tech graduate student Kevin Brenner holds a fabricated graphene sample (courtesy Georgia Institute of Technology).

> The process is the first to provide both electron (N-type) and hole (P-type) doping from a single dopant material.

Researchers elsewhere have demonstrated graphene doping using a variety of processes, including soaking the material in various solutions and exposing it to a variety of gases. Georgia Tech believes its process is the first to provide both electron (N-type) and hole (P-type) doping from a single dopant material. In the process, the doping introduces atoms of hydrogen and oxygen in the vicinity of the carbon lattice. The oxygen and hydrogen do not replace carbon atoms but instead occupy locations atop the lattice structure.

In volume manufacturing, a conventional lithography process would likely replace the e-beam radiation. Varying the reflectance or transmission of the mask set would control the amount of radiation reaching the SOG, and that variation would determine the creation of N- or P-type areas.

"Making everything in a single step would avoid some of the expensive lithography steps," says Murali. "Gray-scale lithography would allow fine control of doping across the entire surface of the wafer."

For doping bulk areas, such as interconnects, that require no patterning, the researchers coat the area with HSQ and expose it to a plasma source. The technique can make the nanoribbons as much as 10 times more conductive than untreated graphene. However, the researchers note that they require a better understanding of how the process works and whether other polymers might provide better results. "We need to have a better understanding of how to control this process because variability is one of the issues that must be controlled to make manufacturing feasible," says Murali. "We are trying to identify other polymers that may provide better control or stronger doping levels."

The Semiconductor Research Corp (www.src.org) and the Defense Advanced Research Projects Agency (www.darpa.mil) through the Interconnect Focus Center (www.ifc.gatech.edu) supported the research, which a paper in *Applied Physics Letters* describes (**Reference 1**).

—by Suzanne Deffree

▷**Georgia Institute of Technology**, www.gatech.edu.

REFERENCE

1 Brenner, Kevin, and Raghunath Murali, "Single step, complementary doping of graphene," *Applied Physics Letters*, Feb 10, 2010, http://scitation.aip.org/vsearch/servlet/VerityServlet?KEY=APPLAB&smode=strresults&sort=chron&maxdisp=25&threshold=0&possible1=Raghunath+Murali&possible1zone=article&OUTLOG=NO&viewabs=APPLAB&key=DISPLAY&docID=1&page=1&chapter=0.

SiGe mixer exhibits low noise, high linearity in wireless base stations

Maxim Integrated Products' new MAX2042 upconverting and downconverting, double-balanced passive mixer operates at 2 to 3 GHz. The SiGe (silicon-germanium) chip includes an internal local-oscillator buffer and two baluns. It outputs an intermediate frequency of 50 to 500 MHz. Power consumption is 690 mW at 5V and 396 mW at 3.3V. Typical applications include LTE (long-term evolution), wireless base stations, WiMax (worldwide interoperability for microwave access), MMDS (multipoint-multichannel-distribution service), and WCS (wireless-communications service).

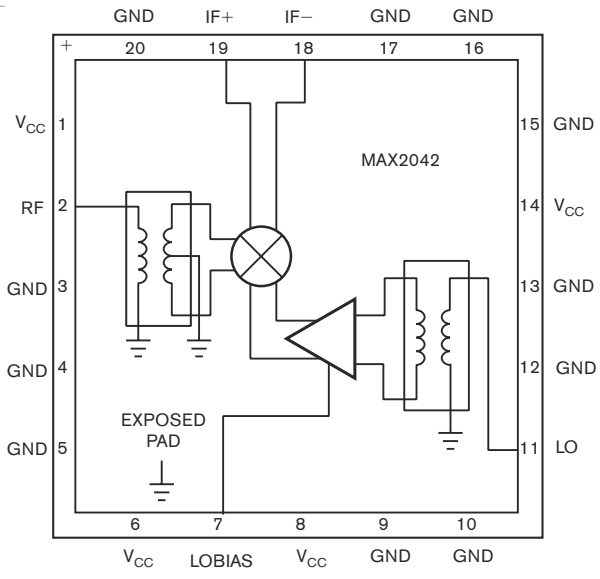
When operating as a downconverter from 5V, the part has a minimum IP3 (third-order intercept point) of 34 dBm (decibels relative to 1 mW). At 3.3V, the typical IP3 is 31 dB. The single-sideband noise figure is 7.3 or 7.5 typical when operating from 5 and 3.3V, respectively. The device's typical small-signal-conversion loss is 7.2 dB at a 3.3 or 5V supply voltage. The second RF harmonic minus the second harmonic of the local oscillator spurs minimum rejection ranges of 54 dBc (decibels relative to the carrier) at 0-dBm output power and a 5V supply to typical rejection of 72 dBm at −10-dBm output power and a 3.3V supply.

When you operate the part as an upconverter, the MAX2042 delivers a minimum IIP3 of 30 dBm at 5V and 29.5 dBm typical at a 3.3V power-supply voltage. The typical small-signal-conversion loss is 6.8 dB for a 3.3 or 5V supply voltage. The unit achieves 67 dBc suppression of the local oscillator plus or minus the second harmonic of the intermediate frequency.

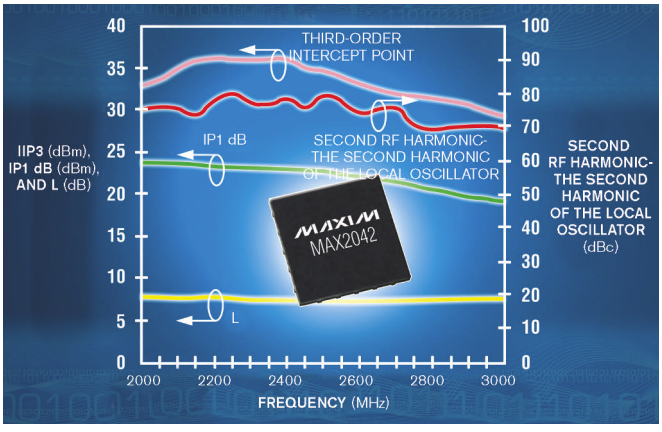
The MAX2042 operates at a −40 to +85°C junction temperature, comes in a 5×5-mm, 20-pin TQFN package, and sells for $5.95 (1000).

—by Paul Rako

▷**Maxim Integrated Products**, www.maxim-ic.com.



The MAX2042 mixer uses a silicon-germanium process to provide good linearity and low noise.

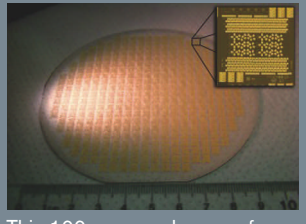


The MAX2042 mixer has integrated baluns and a local-oscillator buffer.

100-mm GRAPHENE WAFERS TARGET NEXT-GENERATION ELECTRONICS

Researchers at the EOC (Electro-Optics Center) at Pennsylvania State University's Materials Research Institute have produced 100-mm-diameter graphene wafers. Using silicon sublimation, EOC researchers David Snyder and Randy Cavalero thermally processed silicon-carbide wafers in a physical-vapor-transport furnace until the silicon migrated away from the surface, leaving behind a layer of carbon that formed into a one- to two-atom-thick film of graphene on the wafer surface.

The researchers are initially focusing on graphene materials to improve transistor performance in various RF applications,



This 100-mm graphene wafer contains approximately 75,000 devices and test structures. The inset shows an optical image of a single chip. Each small square pad on the chip measures 100 microns (courtesy Pennsylvania State University).

with Penn State developing graphene-device processing to enhance graphene-transistor performance. The university has also fabricated RF FETs on 100-mm graphene wafers. The researchers plan to improve the electron mobility of the silicon-sublimated wafers to nearer the theoretical limit, which is approximately 100 times faster than silicon.

The researchers are also using a nonsublimation approach to developing synthesis and device fabrication of graphene on silicon as a means to achieve wafer diameters exceeding 200 mm.—by Suzanne Deffree

▶**Pennsylvania State University Materials Research Institute, www.mri.psu.edu.**

03.18.10

RAQ's

Rarely Asked Questions

Strange stories from the call logs of Analog Devices

Taming A/D Converter Power Supplies

Q. Will a switching power supply (dc-to-dc converter) really degrade the A/D converter's performance?

A. Engineers commonly feel that a switching power supply can degrade the performance of an A/D converter, leading them to choose a low dropout (LDO) linear regulator over a switcher, but this perception isn't entirely true. LDOs have lower ripple and noise specifications, but recent studies show that efficient switchers can be employed in some converter designs provided the designer understands the topology, applies some practical know how, and takes the required precautions.

First choose the converter and then choose the right switcher. Not just any switcher will do. From the datasheet, check the switcher's noise and ripple specifications, as well as its switching frequency. A typical switcher might have 10 µV rms noise over a 100-kHz bandwidth. Assuming the noise is white, this is equivalent to a noise density of 31.6 nVrms/rt-Hz over the band of interest.

Next, check the converter's power supply rejection (PSR) specification to get an understanding of where the converter's performance will degrade due to noise on the supply. 60 dB (1 mV/V) is typical for most high-speed converters over the first Nyquist zone.

Using a 16-bit ADC with 2-Vpp full-scale input range, 78-dB SNR, and 125-MSPS sampling rate, the noise floor is 11.26 n V rms. The noise from any source must be kept below this in order to prevent it from being seen by the converter. In the first Nyquist zone, fs/2, the converter noise will be 89.02 µV rms (11.26 nVrms/

rt-Hz) × sqrt(125 MHz/2). Although the switcher's noise (31.6 nv/rt-Hz) is more than twice that of the converter, remember to account for the converter's 60-dB PSRR, which will suppress the switcher's noise to 31.6 pV/rt-Hz (31.6 nV/rt-Hz × 1 mV/V). This noise is much smaller than the converter's noise floor, so the switcher's noise will not degrade the converter's performance.

Supply filtering, grounding, and layout is important too. Adding 0.1 µF capacitors to the ADC power supply pins will reduce the noise even lower than that calculated above. A simple LC filter on the power supply output may work, but a cascaded filter will suppress the switcher's noise even more. Remember that approximately 20 dB/decade is gained for each additional stage. Tightly stacked power and ground planes (≤4 mil spacing) can add inherent high-frequency decoupling to the PCB design. Lastly, good physical partitioning is key; keep sensitive analog circuits away from switching circuits. For further design assistance with power supplies and converters, contact your local ADI FAE.

To Learn More About How to Power Converters
http://designnews.hotims.com/27739-101

Contributing Writer Rob Reeder is a senior converter applications engineer working in Analog Devices high-speed converter group in Greensboro, NC since 1998. Rob received his MSEE and BSEE from Northern Illinois University in DeKalb, IL in 1998 and 1996 respectively. In his spare time he enjoys mixing music, art, and playing basketball with his two boys.

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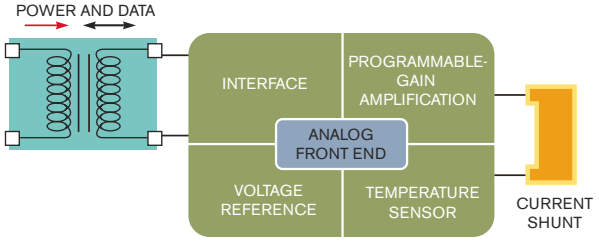
ANALOG DEVICES

Smart power-meter-IC family offers alternative to current transformers

Utility power meters often must rely on a current transformer for polyphase applications. Current transformers have drawbacks, however. They are relatively expensive and require additional copper wiring. Power thieves can also tamper with the devices using large permanent magnets. Shunt current sensors are often simpler and less expensive, but they work only for single-phase, single-element systems. The voltages they measure across phases are too high for the subsequent electronics and also for maintenance personnel (see "Tamper-resistant smart power meters rely on isolated sensors," *EDN*, March 19, 2009, pg 29, www.edn.com/article/CA6643364).



The 71M6541x and 71M6xx1 smart-meter ICs feature digitally isolated current sensors that Teridian based on its proprietary MicroDAA isolation technology.

> The pulse transformer has enough power to energize the sensor IC with accuracy to ANSI 200A Class 0.2.

Teridian takes a different approach to the problem with its new SOC (system-on-chip) smart-metering product family, which includes the 71M6541x and 71M6xx1. The family features digitally isolated current sensors that the company based on its proprietary MicroDAA (data-access-arrangement) isolation technology. The 71M6541x stand-alone meter SOC targets use in single-phase systems. For multiphase systems, designers can eliminate the need for a current transformer and its associated copper wiring by using an inexpensive pulse transformer to interface the 71M6541x to the 71M6xx1 isolated sensor IC, which then connects to a current-sensing shunt element. The 6541 sends a signal to the pulse transformer, which provides a communication signal and has enough power to energize the sensor IC with accuracy to ANSI 200A Class 0.2.

The 71M6541x comes in 64-pin LQFPs with 32- or 64-kbyte flash-memory options; prices start at $2 (10,000). The 71M6xx1 isolated sensors come in eight-pin SOIC packages for prices starting at $1.50 (10,000), depending on current and accuracy range.

—by Margery Conner

▷**Teridian**, www.teridian.com.

CALYPTO TO POWER-MANAGEMENT EXPERTS: HAVE IT YOUR WAY

Calypto Design Systems has for some time now successfully leveraged its core technology–sequential analysis of synchronous logic circuits–into a full suite of tools to reduce power consumption. Analyzing your RTL (register-transfer-level) logic, the Calypto tools identify opportunities to apply fine-grained clock gating and fine-grained use of sleep modes in memory instances. The tools then reorganize the RTL logic if necessary, insert enable signals into the code, and provide a formal equivalence check to make sure they didn't break anything. All of this action takes place before synthesis, during which you in theory still have the most leverage over active and leakage power. The company claims that the tools can reduce power consumption by as much as 60%.

This approach should be great news for teams working on power-constrained designs. Ironically, though, the one group that is in the best position to appreciate what the Calypto tools do–power-management experts–has had an issue: automation. RTL gurus don't want a tool taking liberties with their code, even if it does the right thing. Addressing that issue, Calypto recently announced the PowerAdviser flow, which the company based on Release 3.1 of its PowerPro package. In this flow, the tools analyze your RTL, and PowerAdviser makes recommendations without altering the code.

The flow offers three categories of information in its reports. First, the analyzer generates clock-gate-enable and memory-mode-enable expressions based on your RTL. You can review these expressions at your leisure and drop those that you like directly into your code. This approach is in essence a manual version of the PowerPro CG and MG tools. Second, the analyzer suggests changes to the RTL that would enable further clock- or memory-gating opportunities. For example, the tool might suggest importing a mode-control signal from upstream, making it possible to gate the clock on a register when there is no activity on the block's inputs. If you like PowerAdviser's suggestions, you can modify your RTL and then rerun PowerAdviser, which then generates the correct expressions.

Third, PowerAdviser suggests changes to your microarchitecture that would open up even more gating opportunities. For example, the tool spots registers that rarely change but are not efficiently clock-gated and registers that toggle often in situations in which their outputs don't affect other circuits. You can look into these areas of the design and, if it's appropriate, reorganize them and then return to PowerAdviser to get the enable expressions.

—by Ron Wilson

▶**Calypto Design Systems, www.calypto.com.**

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VOICES

Recognizing technology's inflections

The embedded-processor market is experiencing a lot of activity. Traditional 8- and 16-bit processor vendors are adding small 32-bit processors to their product lineups, and there is a lot of interest in small 32-bit processors, such as the Cortex M3 and M0 processors from ARM. NXP is the lead licensee for the ARM Cortex-M0 core—the most rapidly adopted core in ARM's history. Pierre-Yves Lesaicherre, senior vice president and general manager for NXP Semiconductors' microcontrollers and logic business lines, recently discussed the microcontroller market with *EDN*. An excerpt of that interview follows. For the full text, go to www.edn.com/100318pa.

What is your impression of the current embedded-processor market?

A The embedded market has evolved over the last 30-plus years. Suppliers with proprietary architectures have steadily built positions and niches in many evolving application segments. However, over the last few years, there has been an increasing momentum toward the adoption of the ARM architecture and the ever-widening software and development ecosystem that can be harnessed to speed the development cycle and to reduce development costs. While the 8- and 16-bit markets have stopped growing or are in decline, the 32-bit market is now the fastest-growing segment of the overall microcontroller market. As a result, most microcontroller vendors are now focusing their R&D innovation and marketing effort on new 32-bit solutions, with the ARM architecture gaining increasing importance in the low range to midrange of the 32-bit market.

How and why is the embedded-processor market changing?

A Although the embedded processor was once just the processing engine, we now have differentiated application solutions and more application-centric processors that incorporate all the peripherals and resources required for a certain application or vertical segment of the market, such as e-metering, white goods, motor control, and medical. In addition, the software development and infrastructure have become major drivers and key decision factors in customer project and life cycle. Embedded developers often value a strong ecosystem and support infrastructure as importantly as the performance of the microcontroller when making their processor and vendor selection.

What applications are most affecting or affected by these emerging changes?

A Most industrial applications connected to energy efficiency, renewable energy, metering, motor and power control, and sensor interfacing are moving from bit-oriented control solutions—that is, 8 bits—toward math-intensive, graphical, and touch-controlled user interfaces. There is a growing need for much more interconnected control between units and nodes and within the home, building, and factory floors. With R&D budgets stagnating or even decreasing and shortening time-to-market requirements, embedded developers look for processors that better fit the needs of their applications, and they have to rely on a strong ecosystem, support, and infrastructure to speed up their development and keep innovation costs at a reasonable level.

How do you see development tools maturing and changing?

A The customer base for the embedded space is expanding. A single development environment can no longer meet the demands of this fragmented user base. For instance, NXP sees four distinct groups of users we need to serve. [First are] the traditional embedded developers. These customers are well-served by the traditional tool manufacturers, such as Keil, IAR, and others. The customers are highly skilled in the art of writing embedded code and take great pride in building the most out of everything a microcontroller has to offer, even if it means getting down to the bits, bytes, and register-level details.

[The second group is] the open-source environment. This group of customers is used to the do-it-yourself method of embedded-application development. These customers are fiercely loyal to the community and have propelled the progress of IDEs such as Eclipse, operating systems such as Linux, and compilers such as GNU and LLVM.

[The third group is the engineers who need] fast-prototype, proof-of-concept tools. Embedded engineers struggle to provide a streamlined way of taking an idea all the way to a demonstration to show the merit of the idea to their marketing or management team. Code size and perfecting the code are top priorities at this stage. A tool such as mbed [www.mbed.org] takes embedded programming a few levels higher: building C/C++ libraries on top of device drivers and exposing the users to a high-level API [application-programming-interface]-driven tool that's clean and easy to use.

[The last group comprises] PC programmers. With the microcontroller manufacturers providing extremely capable devices with large memory and high performance at very low prices, a new group of users has entered the embedded space.**—interview conducted and edited by Robert Cravotta**

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34410A	6 ½	0.0030%	10,000 / sec	2.6 ms	GPIB, USB, LAN (LXI)
34411A/ L4411A	6 ½	0.0030%	50,000 / sec	2.6 ms	GPIB, USB, LAN (LXI)
34420A	7 ½	0.0030%	250 / sec	.02 sec	GPIB, RS-232
3458A	8 ½	0.0008%	100,000 / sec	3.0 ms	GPIB

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BY BONNIE BAKER

System or technology dictates ADC choice

How do you decide which ADC technology to use in your applications before you do a thorough system evaluation? Maybe you prefer SAR (successive-approximation-register) ADCs because you assume they are easy to use and a bit faster than delta-sigma converters. Then again, you may select delta-sigma converters because you assume they are slower but have good resolution. What the heck? Maybe you choose the ADC that you have always used.

When selecting a converter, you usually base your decision on the ENOB (effective number of bits); accuracy; repeatability, or noise; and output data rate. You may assume that SAR ADCs produce accurate outputs with medium output speeds and that delta-sigma converters produce lower-noise output signals with slower output data rates. These assumptions may no longer guide you when deciding between a SAR ADC and a delta-sigma ADC.

Think about changing your design paradigm from focusing on individual devices to considering the complete system. You will find that both ADC architectures might be appropriate for a given application. For instance, if you know the system ENOB, you may find that combining an analog gain stage with a SAR ADC matches the performance of a higher-speed delta-sigma converter.

A system evaluation includes inspecting the system's sampling speeds, analyzing its accuracy, and comparing its repeatability, or noise-level, capability. To inspect sampling speeds, select a single clock frequency and allow time for the analog components to fully settle before conversion. With system accuracy, you combine the dc performance characteristics into a total-unadjustable-error figure of merit for comparison.

The repeatability evaluation differs from the accuracy evaluation in that it defines how consistently a value from one conversion to the next repeats itself. With a repeatability evaluation, you can combine the noise performance of the signal-chain devices in terms of effective resolution.

As we examine the accuracy and repeatability in our system evaluations, we will use **Table 1** as our starting point. The circuits in the **table** encompass handheld-meter, data-logger, automotive-system, monitoring-system, and many other applications. Each system's gain ranges from one to 128. Column 2 in the **table** lists the ideal system's full-scale range referred to the input of the system. The system's LSB (least-significant bit, Column 3) is equal to the system's full-scale range divided by the number of system codes: 4096.

In my next column, I'll delve into the conversion speeds of these designs. In future columns, I'll examine the differences between a 12-bit SAR ADC, a multiplexed PGA (programmable-gain-amplifier)-SAR ADC, and a 24-bit multiplexed delta-sigma converter. The analog or digital gain range for each system will be 1 to 128V/V, and the power-supply voltage will be 5V. I'll also investigate the accuracy and repeatability of these systems.

Here is the trillion-dollar question: Which system is best for the listed applications—a PGA-SAR ADC or a delta-sigma ADC? You can reach me at ti_bonniebaker@list.ti.com with your best guess. Be sure to include a description of your application with its basic requirements. EDN

TABLE 1 ADC COMPARISON

Analog or process gain	Full-scale range (V, referred to input)	LSB (µV, referred to input)
One	5	1220.7
Two	2.5	610.35
Four	1.25	305.18
Eight	0.625	152.59
16	0.3125	76.29
32	0.1563	38.15
64	0.0781	19.07
128	0.0391	9.54

REFERENCES

1 Baker, Bonnie C, "Analog-to-Digital Converters, Part 4 of 6: Move Your System Strategy to the Forefront in Your ADC Designs," Texas Instruments, Dec 3, 2009, www.en-genius.net/includes/files/acqt_113009.pdf.
2 "Nuts and Bolts of the Delta-Sigma Converter," Texas Instruments, www.ti.com/nutsandboltsvideo-ca.

Bonnie Baker is a senior applications engineer at Texas Instruments and author of A Baker's Dozen: Real Analog Solutions for Digital Designers.

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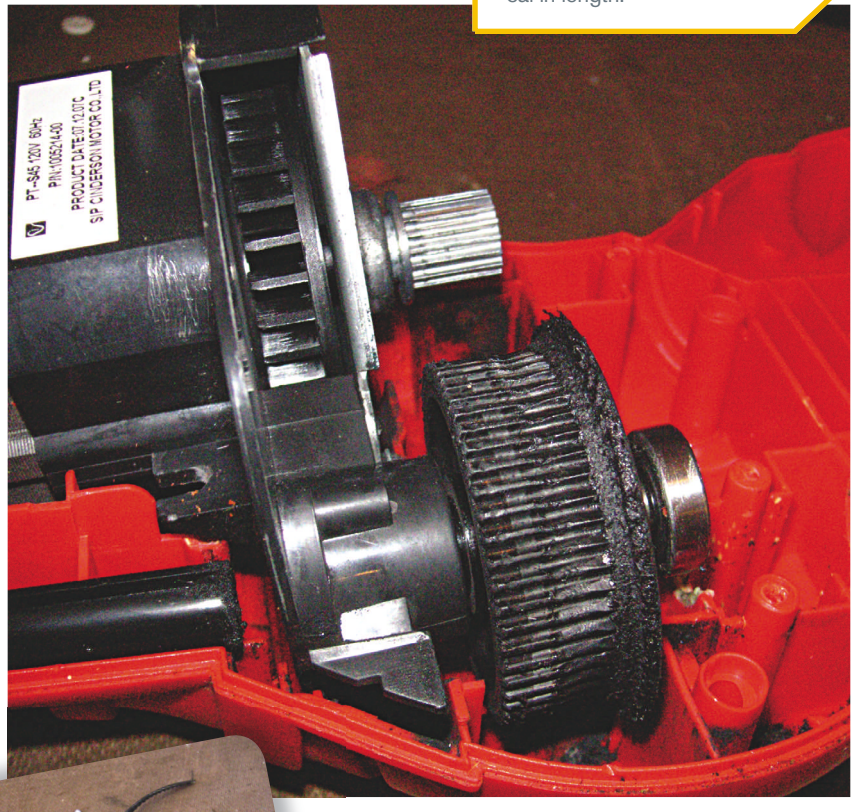
The Black and Decker GH1000 Type 2 string trimmer

After my disappointment with the performance of string trimmers with 0.040- and 0.065-in. strings, I bought a futuristic-looking Black and Decker model that used professional-size 0.080-in. line. Around the end of the two-year warranty period, the string stopped spinning, even though the motor was still turning. Prying into the interior, I saw that the drive belt had broken and the drive pulley had melted. I replaced the belt with a $7 belt from eReplacementparts.com. Although the company sells the aluminum drive pulley for only $1.42, it does not offer the plastic drive pulley. I spent an hour and still couldn't figure out how to disassemble the drive pulley. I did make sure I got a spare belt; the new one won't last long.

The manufacturer used several holes for fixturing during factory assembly. All the screws holding the case halves together are identical in length.

SIP Cinderson of Suzhou, China—near Shanghai—makes the universal brushed motor rated at 120V and 7.2A. It has a nominal power consumption of 874W, or about 1 hp.



Inadequate structure between the motor and the drive pulley means that the cogged belt will run off the pulleys under heavy loads, such as when you are cutting thick weeds and grass.

The designers added a large flange on the driven pulley to keep the belt from flying off. They also lengthened the drive pulley to keep the belt engaged as it tries to run off the drive pulley.

Although the flange on the drive pulley prevents the belt from flying off, the side pressure creates enough friction to melt the plastic. The molten plastic solidified under the belt, eventually causing it to rip apart.

The designers covered a screw with a decal, making disassembly frustrating. Other than this problem, the design follows good Z-axis assembly practices. You can put every subassembly onto the bottom half of the case, then put on the top half and screw it together all from one direction, the Z axis.

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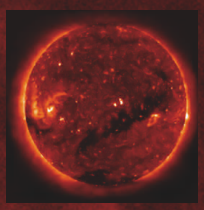

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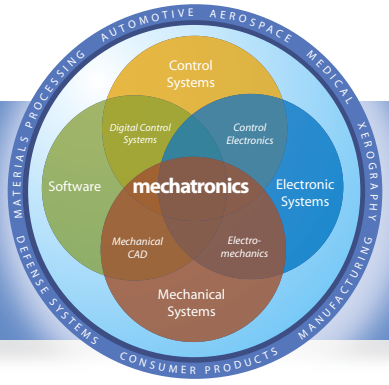
MECHATRONICS IN DESIGN

FRESH IDEAS ON INTEGRATING MECHANICAL SYSTEMS, ELECTRONICS, CONTROL SYSTEMS, AND SOFTWARE IN DESIGN



Analogies give engineers insight

Insight based on fundamentals is the key to innovative multidisciplinary problem-solving.

A person trying to explain a difficult concept will often say, "Well, the analogy is … ." The use of analogies in everyday life aids in understanding and makes everyone better communicators. Mechatronic systems depend on the interactions among mechanical, electrical, magnetic, fluid, thermal, and chemical elements, and most likely combinations of these. They are truly multidisciplinary, and the designers of mechatronic systems are from diverse backgrounds. Knowledge of physical system analogies can give design teams a significant competitive advantage.

Consider the exhaust system of a motorcycle and its heat shield. Temperatures have to be controlled through design for performance but also to protect the rider. Being able to model this system as a network of thermal resistances and capacitances, just like an electrical circuit, is a powerful design tool. It allows the engineer to visualize the flow of heat and the storage of thermal energy and specify key temperatures by selection of materials and geometries that vary the network thermal resistances (conduction, convection, and radiation) and capacitances. Improving performance happens with understanding—not by trial and error—and quickly.

Kevin C Craig, PhD, is the Robert C Greenheck chair in engineering design and a professor of mechanical engineering, College of Engineering, Marquette University. For more mechatronic news, visit mechatronicszone.com.

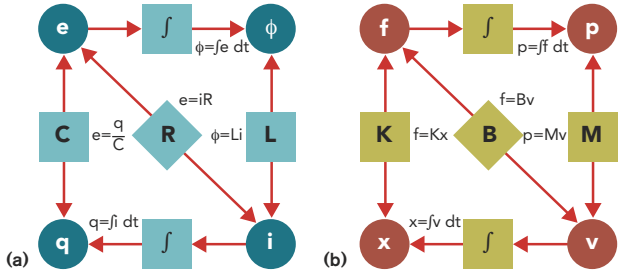


Figure 1 The model structures for electrical systems (a) and mechanical systems (b) display an obvious analogy.

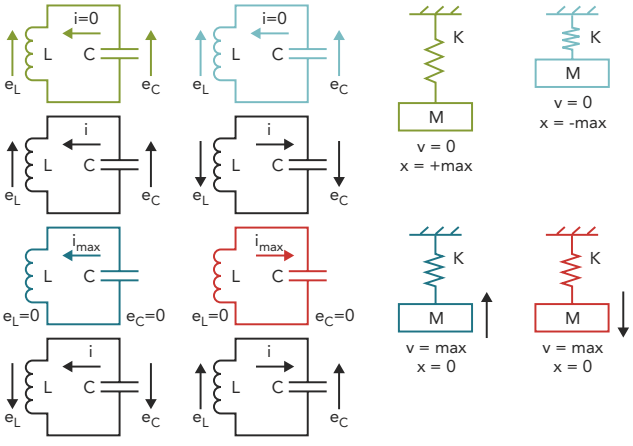


Figure 2 Colored system diagrams correspond to each other.

To explore in some depth the nature of physical system analogies, let's use the common electrical-mechanical analogy. These systems are modeled using combinations of pure (only have the characteristic for which they are named) and ideal (linear in behavior) elements: resistor (R), capacitor (C), and inductor (L) for electrical systems, and damper (B), spring (K), and mass (M) for mechanical systems. The variables of interest are voltage (e) and current (i) for electrical systems and force (f) and velocity (v) for mechanical systems. **Figure 1** shows the model structures for these systems. The analogy is obvious!

We can use this analogy to explain the flow of current and the changes in voltages in an LC (inductor-capacitor) electrical circuit—difficult to envision for most mechanical engineers and even for some electrical engineers—by comparing it with a spring-mass mechanical system. **Figure 2** is color-coded: Colored diagrams for each system correspond to each other. By comparing the motion of the mass—its changing potential energy corresponding to energy stored in the electric field of the capacitor and its changing kinetic energy corresponding to energy stored in the magnetic field of the inductor—one can better understand how electrical capacitors and inductors function.

For enhanced multidisciplinary engineering system design and better communication and insight among the design team members, the use of analogies is a powerful addition to an engineer's toolbox. EDN

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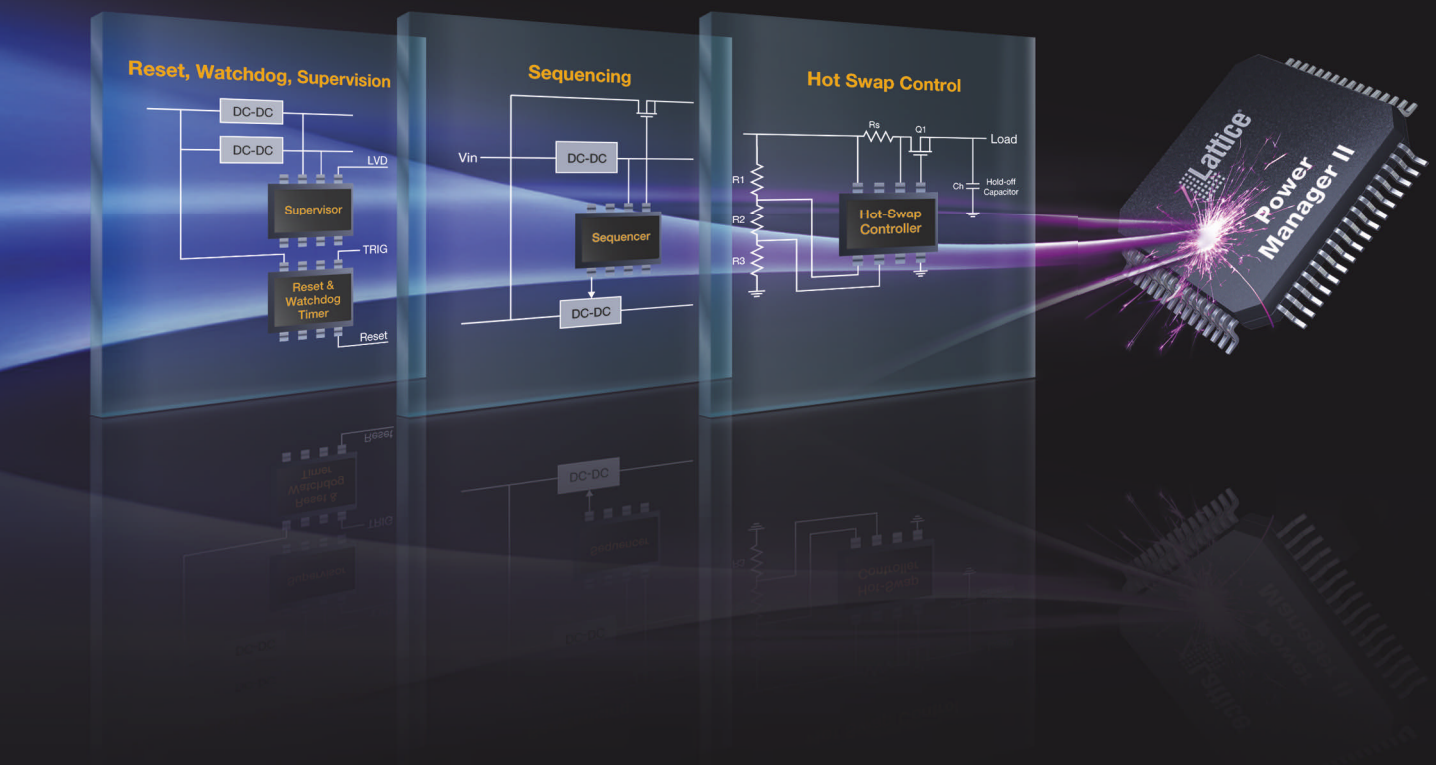

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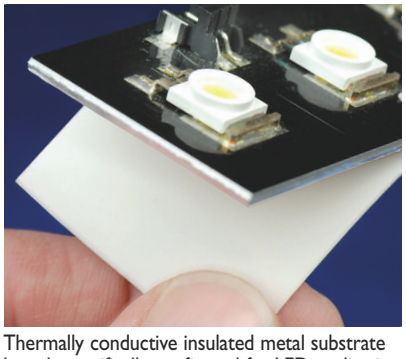

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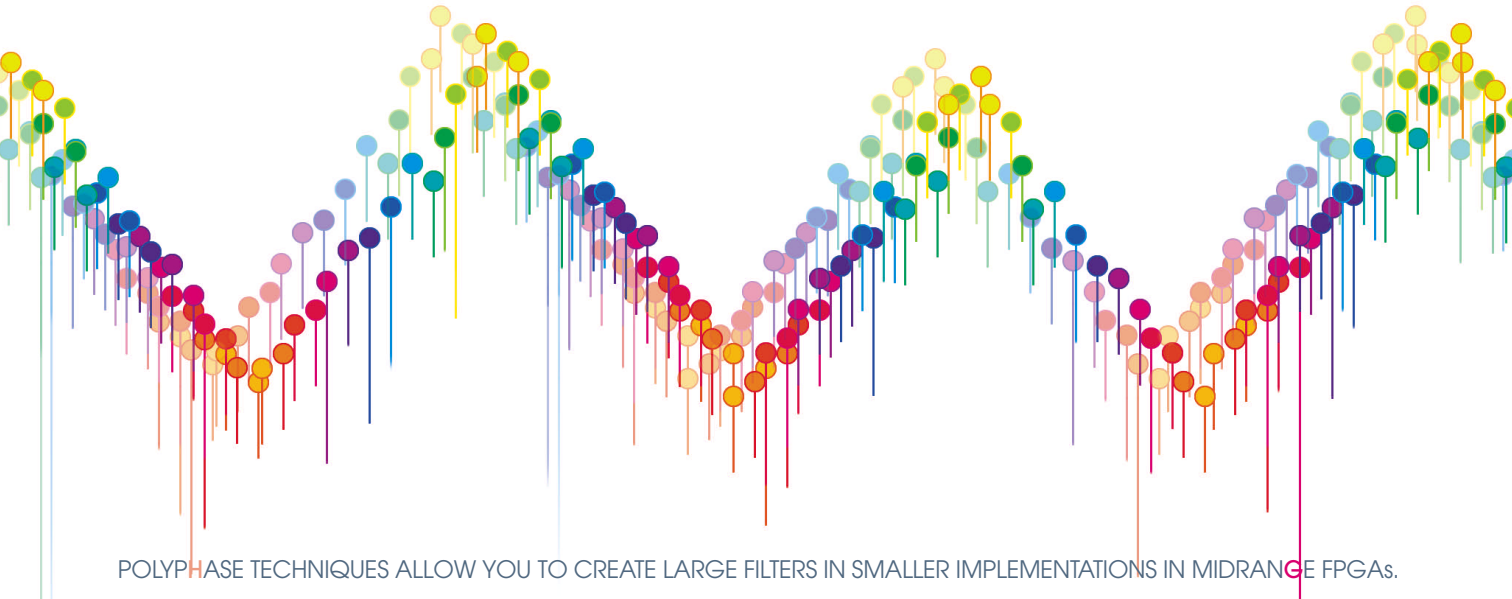

POLYPHASE TECHNIQUES ALLOW YOU TO CREATE LARGE FILTERS IN SMALLER IMPLEMENTATIONS IN MIDRANGE FPGAs.

POLYPHASE FILTERS REDUCE SATURATION

BY RON WARNER • LATTICE SEMICONDUCTOR CORP

Digital signal processing is ubiquitous in modern electronic systems, from MP3 players to digital cameras to wireless handsets. One of the mainstays of a DSP designer's tool box is the FIR (finite-impulse-response) filter. The longer the FIR filter—that is, the greater the number of taps—the better the filter's response. This situation involves a trade-off, however, because more taps require increased logic requirements, increased computational complexity, increased power consumption, and a greater potential for saturation or overflow.

Designers can employ polyphase techniques to implement filters that provide comparable results and use less logic, requiring fewer computational resources, consuming less power, and having less potential for saturation and overflow. The resulting filters fit into today's new class of smaller, midrange FPGAs.

SOME SAMPLING THEORY

A multirate system uses multiple sampling rates. In some cases—for example, conversion of professional audio into consumer CD-quality audio—a system may sample a signal at one rate, and another portion of the system, operating at a different rate, needs the signal. In this case, you must increase or decrease the sampling rate of the original signal as necessary. Alternatively, the data's original sample rate may be higher than an application requires. Thus, reducing the sample rate and then operating on the resulting data can dramatically decrease data-throughput requirements, reduce memory requirements, increase processing efficiency, and reduce power consumption.

Let's first consider the problem of reducing the sample rate. Assume that your system originally sampled a signal at a frequency, F (**Figure 1**). Now assume that you want to reduce the sample rate to one-fourth of the original frequency. One way of achieving this reduction would be to simply throw away three of every four of the original samples (**Figure 2**). If you were to discard some samples, the resulting signal could contain aliasing artifacts. In the context of digital signal processing, "aliasing" refers to an effect that causes continuous signals to become indistinguishable from each other after sampling; that is, they become aliases of one another. "Aliasing" also refers to the distortion or artifacts that occur when a signal reconstructed from samples differs from the original continuous signal.

For example, consider an audio signal, such as music, that may contain inaudible high-frequency components. If you sample this signal at too low a rate, which is effectively what you are doing when you discard some samples, and then reconstruct the music with a DAC, you may hear the low-frequency aliases of the undersampled high-frequency components. To avoid this problem, you typically remove the unwanted high frequencies with a lowpass filter before discarding the unwanted samples (**Figure 3**).

Generally speaking, "downsampling" refers only to the process of discarding samples without performing the filtering operation. By comparison, "decimation" refers to the process of reducing the sample rate—that is, performing the filtering operation and then discarding the samples. In practice, the terms "downsampling," "downconversion," and "decimation" are often interchangeable. The "decimation factor," M, refers to the ratio of the input sampling rate to the output sampling rate. In this example, the input rate is four times the output rate, so M=4.

Consider a situation in which you want to increase the sample rate. The typical reason for doing so is to enable another portion of the system operating at a higher sample rate to work with the signal. Suppose that you start with a signal that the system originally sampled at frequency F (**Figure 4**). Now assume that you want to increase the sample rate to four times the original frequency. You start by inserting zero-value samples between the original samples to increase the sampling rate (**Figure 5**). This approach creates a problem, however, because the new zero-value samples add unwanted spectral components to your signal. To solve this problem, you filter the new signal to remove the undesired components and to generate more appropriate sample values (**Figure 6**).

Technically, "upsampling" refers only to the process of inserting the zero-value samples. By comparison, "interpolation" refers to the process of increasing the sample rate—that is, inserting the zero-value samples and then performing the filtering operation. This DSP form of interpolation differs from the classic mathematical-interpolation methods for constructing new data points from existing data points, but it's conceptually the same in that it involves generating new values from existing values. In practice, the terms "upsampling," "upconversion," and "interpolation" often are interchangeable.

"Interpolation factor," L, refers to the ratio of the output sampling rate to the input sampling rate. In this example, the output rate is four times the input rate, so L=4 (**Figure 7**). Note that decimation and interpolation factors can assume only integer values. That is, you can decimate or interpolate only by integer factors, not by fractional factors. In the case of decimation, for example, you can discard only an integer number of samples—that is, one of two, one of three, two of three, three of four, and so forth.

Assume that you want to modify the sample rate of a signal to interface it between two subsystems. If the ratio of the sample rates of the subsystems is an integer value, then you need only perform decimation or interpolation. However, if the ratio of the sample rates is a fractional value, then you must perform resampling, a combination of decimation and interpolation. For example, to resample by a factor of 2.5, you would first interpolate by a factor of five and then decimate by a factor of two to produce an output with a sampling rate of 5/2=2.5 that of the input sampling rate

AT A GLANCE

- In the context of digital signal processing, "aliasing" refers to an effect that causes continuous signals to become indistinguishable from each other.
- Decimation and interpolation factors can assume only integer values—that is, you can decimate or interpolate only by fractional factors.
- Digital filters are typically either FIR (finite-impulse-response) or IIR (infinite-impulse-response) types.
- FIR filters offer several advantages over IIR filters, including the fact that they have completely constant group delay throughout the frequency spectrum and they exhibit complete stability at all frequencies.

TABLE 1 SAMPLE DECIMATION IMPLEMENTATIONS

	Conventional eight-tap FIR filter	Polyfilter 1 with four two-tap subfilters	Polyfilter 2 with one two-tap subfilter
No. of multipliers	Eight	Eight	Two
No. of adders	Eight	Nine	Three
No. of multiplying operations per master clock	Eight	Two	Two
No. of addition operations per master clock	Eight	Three	Three

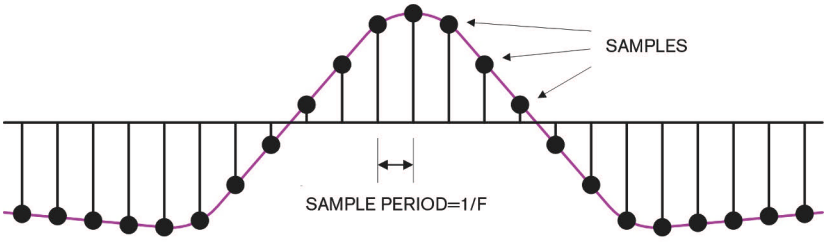

Figure 1 The original signal has a sample rate of F Hz.

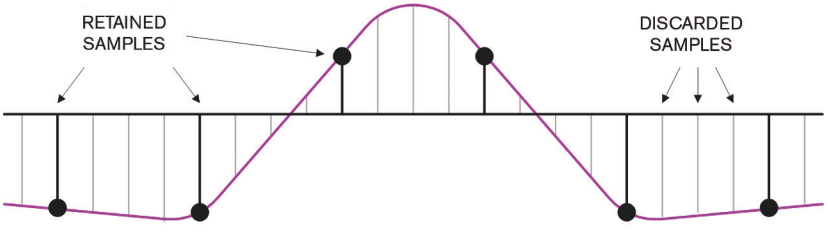

Figure 2 The new signal has a sample rate of F/4 Hz.

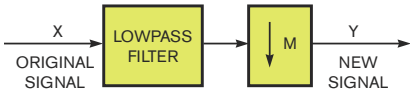

Figure 3 You must filter the signal before discarding any samples.

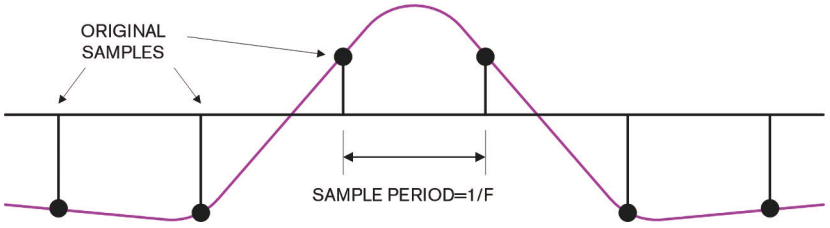

Figure 4 The original signal has a sample rate of F Hz.

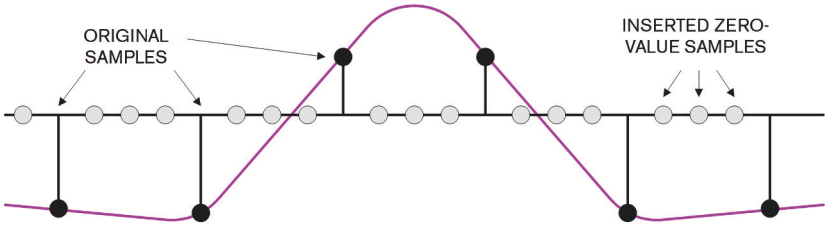

Figure 5 You can augment the original signal with zero-value samples.

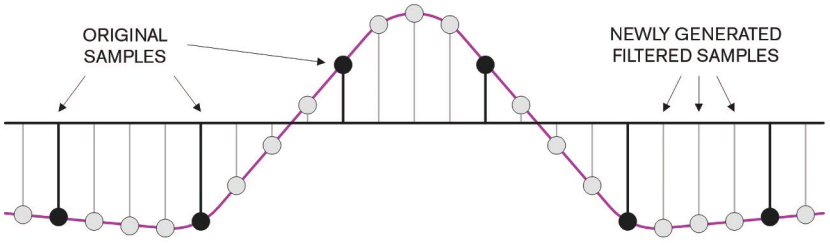

Figure 6 The final signal has a sample rate of 4×F Hz.

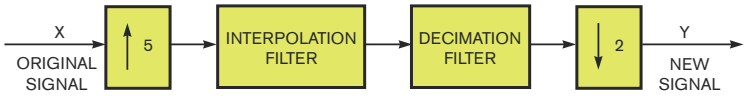

Figure 8 In the resampling, the interpolation factor, L, is five and the decimation factor, M, is two.

Figure 9 In a resampling of professional to commercial audio, L=147 and M=160.

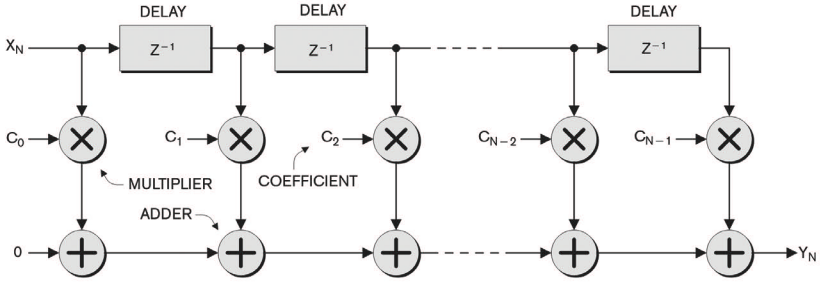

Figure 10 In a generic FIR filter, the input samples, X_N, pass through a series of buffer registers, Z^{-1}, corresponding to the Z-transform representation of a delay element.

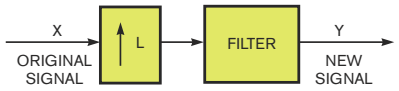

Figure 7 You filter the signal after inserting zero-value samples.

(**Figure 8**). In practice, this approach combines the interpolation and decimation filters in **Figure 8**. The term "resampling factor" refers to the ratio between the output sampling rate and the input sampling rate. Regardless of the frequencies involved, you can express this figure as the ratio between the interpolation and decimation factors, L/M, which is 5/2=2.5 in this case.

As another example, consider the process of resampling a professional audio signal captured at a sample rate of 48 kHz for use in consumer audio equipment requiring a sample rate of 44.1 kHz. In this case, the resampling factor equals the ratio of the output rate to the input rate: 44.1 kHz/48 kHz=0.91875 kHz. Looking at this another way, you must change the sampling rate from 48,000 Hz to 44,100 Hz, which means that the output-to-input ratio is 44,100/48,000=441/480=147/160 kHz. Because 147 and 160 have no common factors, you must stop at this point, which means that you must interpolate by a factor of 147 and then decimate by a factor of 160 (**Figure 9**).

Once again, you can express the resampling factor as the ratio between the interpolation and the decimation factors, L/M, which is 147/160=0.91875. Not surprisingly, this value is exactly the same as the one you obtained from the ratio of the output and input sampling rates because you derived the required interpolation and decimation factors from these rates.

INTRODUCING FIR FILTERS

Digital filters are typically either FIR or IIR (infinite-impulse-response) types. IIR filters use feedback and tend to mimic the response of traditional analog filters. The use of feedback means that their impulse response is recursive and extends over an infinite period of time. Although they require fewer computations than FIR filters, IIR filters may have stability issues, and they cannot match the performance of FIR

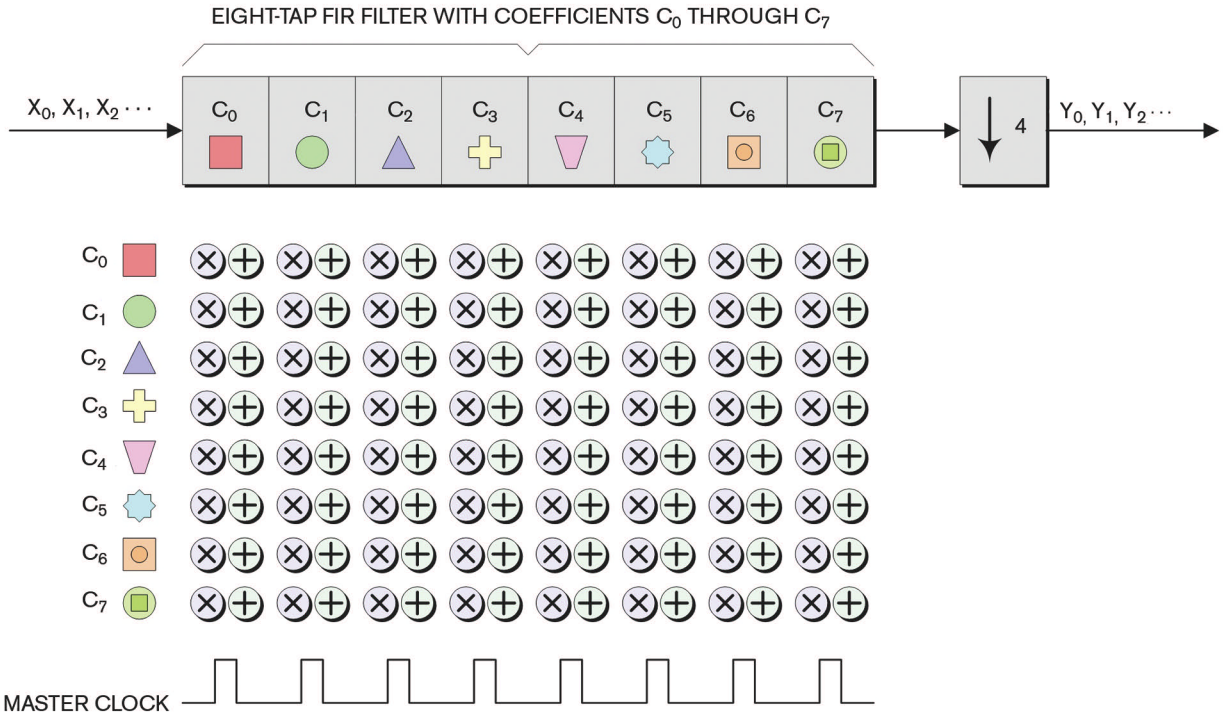

Figure 11 In a symbolic representation of a decimation subsystem using a conventional eight-tap FIR filter, assume a decimation factor of four and assume that the master clock is running at some frequency.

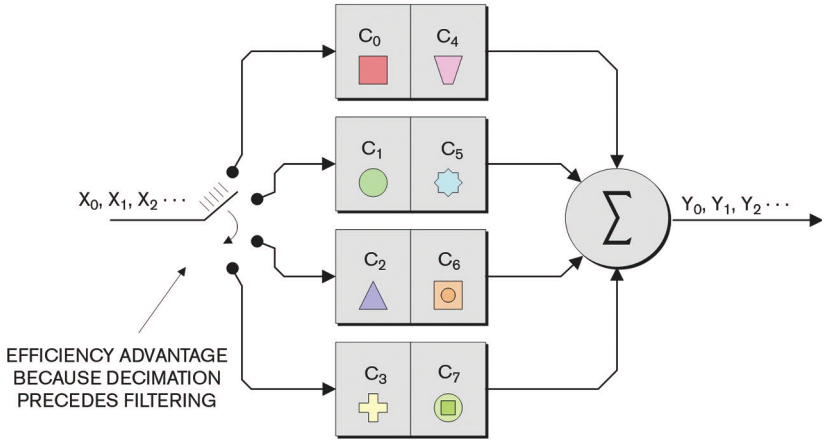

Figure 12 In a polyphase implementation, you could split your original eight-tap FIR filter into four two-tap subfilters.

filters. In comparison, a FIR filter has no feedback, which means that its impulse response lasts for a finite duration of time. FIR filters offer several advantages over IIR filters, including the fact that they have completely constant group delay throughout the frequency spectrum and they exhibit complete stability at all frequencies, regardless of the size of the filter.

In a generic FIR filter, the input samples, X_N, pass through a series of buffer registers, Z^{-1}, corresponding to the Z-transform representation of a delay element (**Figure 10**). The filter works by multiplying an array of the most recent N data samples by an array of constants, or tap coefficients, and summing the elements of the resulting array. By varying the weights, or values, of the coefficients and the number of filter taps, a FIR filter can realize virtually any desired frequency-response characteristic. The problem is that a FIR filter may require hundreds of taps to achieve its desired goal. Each tap requires a MAC (multiply/accumulate) unit, which consumes logic resources. Also, each tap performs a multiplication operation and an addition operation on every clock, which consumes power.

PERFORMING DECIMATION

The underlying concept of polyphase filters is to split a FIR filter into a number of smaller elements and to then combine the results from these elements. First, consider a symbolic representation of a decimation subsystem using a conventional eight-tap FIR filter (**Figure 11**). Assume a decimation factor of four and assume that the master clock is running at some frequency, F. As usual, you discard any unwanted samples after the filtering operation has taken place,

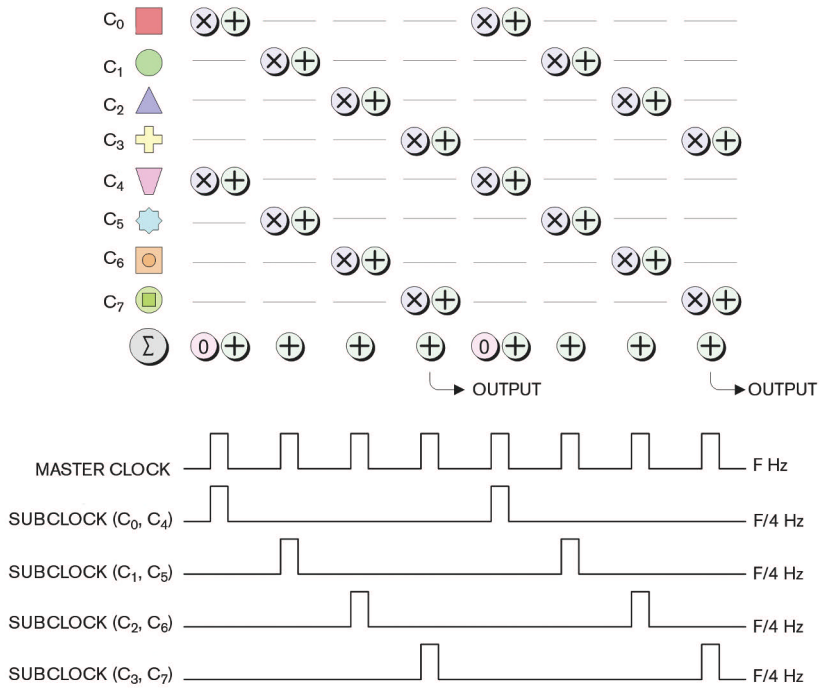

Figure 13 Each of the four subfilters is effectively running at a frequency of F/4 Hz.

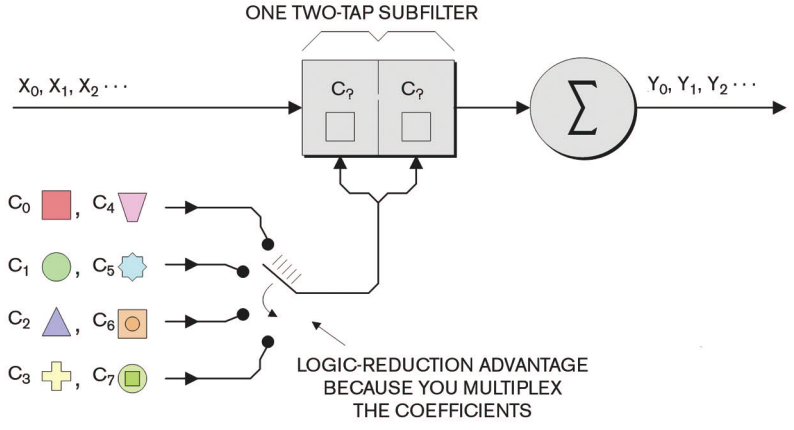

Figure 14 You use each of the four subfilters in this initial polyphase implementation only one-fourth of the time, so you require only one of them at any time, which leads to a slightly more refined implementation.

TABLE 2 SAMPLE INTERPOLATION IMPLEMENTATIONS

	Conventional eight-tap FIR filter	Polyfilter 1 with four two-tap subfilters	Polyfilter 2 with one two-tap subfilter
No. of multipliers	Eight	Eight	Two
No. of adders	Eight	Eight	Two
No. of multiplying operations per master clock	Eight	Two	Two
No. of addition operations per master clock	Eight	Two	Two

but this approach is inefficient because it means that you are performing the filtering at the full clock frequency. In other words, every tap stage performs a multiplication and an addition on every clock. In comparison, in a polyphase implementation, you could split your original eight-tap FIR filter into four two-tap subfilters (**Figure 12**).

Assuming that the same master clock runs at some frequency, F, you can visualize the input data stream as feeding into a rotating switch, which you would implement using standard logic techniques. You feed the first data value to the first subfilter, the second data value to the second subfilter, the third data value to the third subfilter, and the fourth data value to the fourth subfilter. You then loop around so that you feed the fifth data value to the first subfilter, the sixth data value to the second subfilter, and so on.

Using subfilters reduces the potential for saturation and overflow. You typically handle any saturation or overflow that might occur only in the final summing function. In addition, using subfilters provides an immediate efficiency advantage because you are effectively decimating the data before performing the filtering operation. It also means that each of the four subfilters is effectively running at a frequency of F/4 Hz (**Figure 13**).

In addition to any registers and general-purpose logic, each tap in a conventional eight-tap FIR filter contains a multiplier and an adder, which yields a total of eight multipliers and eight adders. Some additional logic following the filter is also necessary to discard any unwanted samples. Similarly, each tap in the initial four-by-two-tap polyphase implementation contains a multiplier and an adder, which yields a total of eight multipliers and eight adders. The amount of logic necessary for implementing the rotating switch feeding the filters in the polyphase implementation is roughly equivalent to the logic necessary for discarding the unwanted samples in the conventional eight-tap FIR filter. The polyphase implementation also requires some additional logic and an adder to accumulate the results from the four subfilters. Thus, the end result is that this initial polyphase implementation requires a little more logic than does a conventional eight-tap FIR filter.

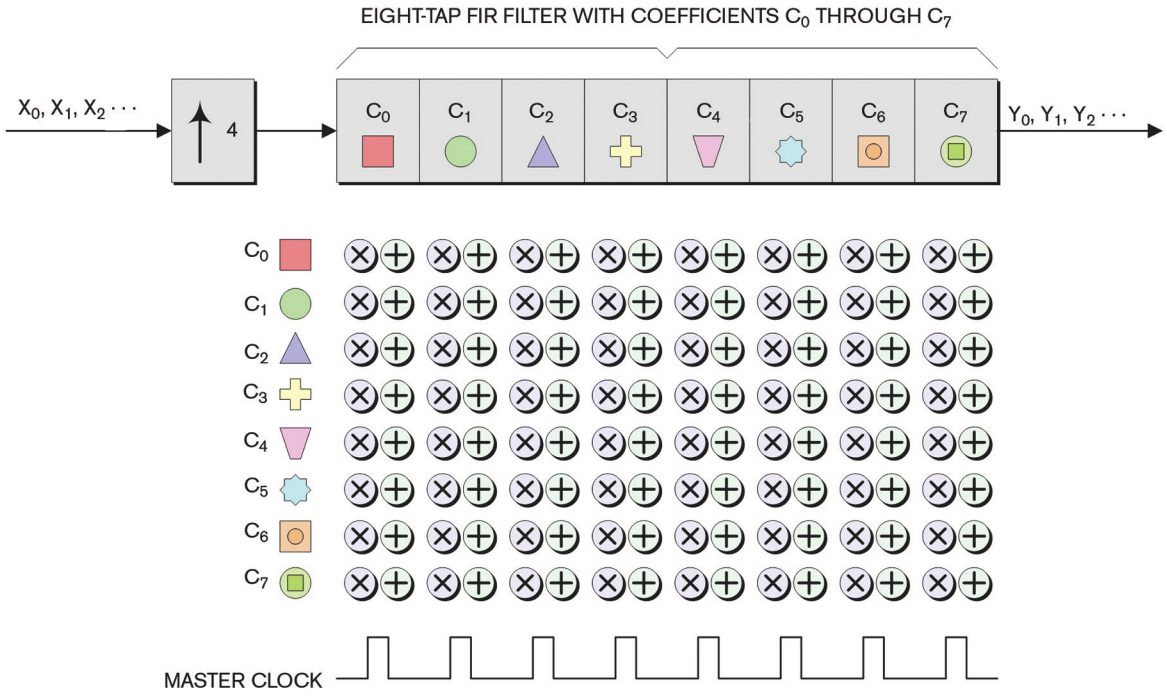

Figure 15 In a symbolic representation of an interpolation subsystem employing a conventional eight-tap FIR filter, assume an interpolation factor, L, of four and a master-clock frequency.

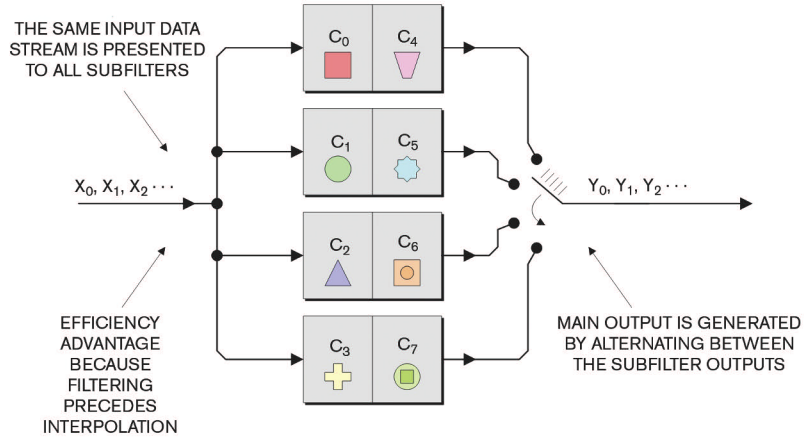

Figure 16 In a polyphase implementation in which you partition the original eight-tap FIR filter into four two-tap subfilters, the same input data stream enters all four subfilters, and you generate the main output data stream by alternating between the subfilter outputs.

However, a conventional eight-tap FIR filter must perform eight multiplications and eight additions on every clock. In comparison, the polyphase implementation has only one active subfilter on any main clock. In this example, each subfilter contains two taps, meaning that the filter portion of this function performs only two multiplications and two additions on each clock.

The summing function that gathers the results from the four subfilters also must perform an addition on each main clock. You clear this accumulator to zero at the beginning of each four-clock cycle. The accumulator then gathers the results from the four subfilters and outputs a new value at the end of each four-clock cycle. Each of the subfilters in the initial polyphase implementation is then effectively running at one-fourth the frequency of its counterpart in a conventional eight-tap FIR filter. Thus, the initial polyphase implementation in turn performs only two multiplications and three additions, including the addition that the summer performs, on each master clock, which results in significant power savings. Also, you use each of the four subfilters in this initial polyphase implementation only one-fourth of the time, so you require only one of them at any time, which leads to a slightly more refined implementation (**Figure 14**).

In this case, you employ a two-tap subfilter, in which each tap contains a multiplier and an adder. On each master clock, you select the appropriate pair of coefficients. Each tap would also require additional registers and logic to maintain context, but this addition is negligible when you consider the reduction in multipliers and adders versus the initial

polyphase implementation. You still perform only two multiplications and three additions on each master clock in the polyphase implementation (**Table 1**).

PERFORMING INTERPOLATION

Consider a symbolic representation of an interpolation subsystem employing a conventional eight-tap FIR filter (**Figure 15**). For the purposes of these examples, assume an interpolation factor, L, of four and a master-clock frequency, F. The upsampling—that is, the process of inserting zero-value samples—takes place before the filtering operation.

Now consider an initial polyphase implementation in which you partition the original eight-tap FIR filter into four two-tap subfilters (**Figure 16**). In this case, the same input data stream enters all four subfilters, and you generate the main output data stream by alternating between the subfilter outputs. The end result is that this polyphase implementation contains the same number of multipliers and adders as does the conventional eight-tap FIR filter. However, because you filter before you interpolate, the subfilters must run at only one-fourth the master-clock frequency, which results in significant power savings. The master clock samples between the subfilter outputs.

Also, the polyphase implementation requires no upsampling logic, and you could replace the original polyphase-filter implementation with one using a single two-tap subfilter running at the full master-clock frequency and multiplexing the coefficients (**Table 2**).

In short, you can use polyphase techniques to implement filters that provide comparable results and use less logic, requiring fewer computational resources, consuming less power, and having less potential for saturation and overflow. Polyphase-filter-based decimators, interpolators, and resampling functions are thus ideal for use with smaller midrange FPGAs. Features such as dual-slice architectures and the ability to cascade or chain DSP slices and blocks, available in some new FPGA architectures, make these devices ideal for conventional FIR- and polyphase-based filtering. EDN

POLYPHASE-FILTER-BASED DECIMATORS, INTERPOLATORS, AND RESAMPLING FUNCTIONS ARE IDEAL FOR USE WITH SMALLER MIDRANGE FPGAs.

AUTHOR'S BIOGRAPHY

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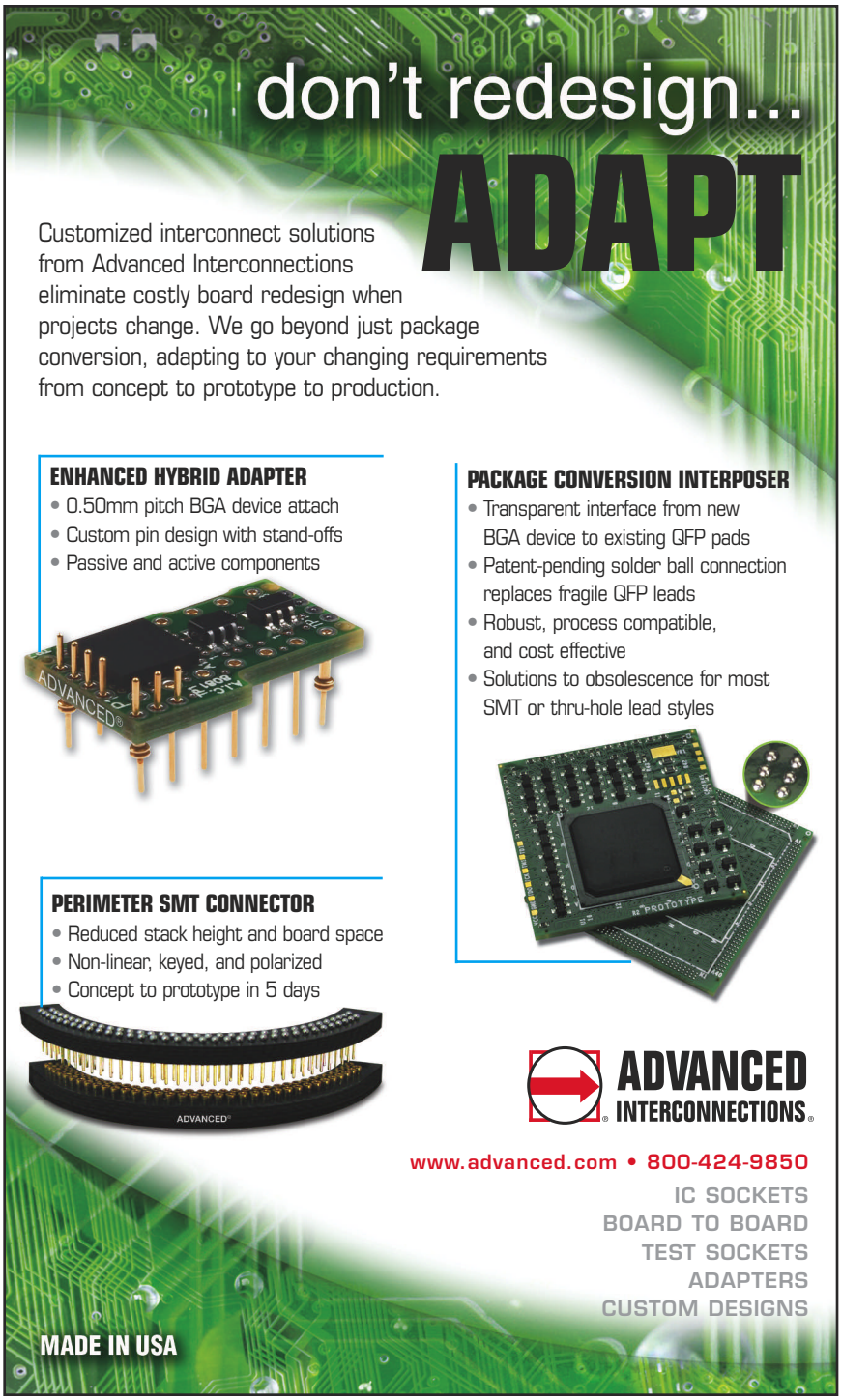

SIGNAL-INTEGRITY PROBLEMS CAN COME BACK TO BITE YOU IF YOU'RE NOT CAREFUL. SPECIALIZED SOFTWARE KEEPS THE SHARKS AWAY.

BY PAUL RAKO • TECHNICAL EDITOR

SWIMMING *in* THE CHANNEL

CHIP AND SYSTEM-INTERFACE DESIGN changed radically when electronic systems began to use high-speed serial channels. Serial links in high-speed buses, such as SERDES (serializer/deserializer), DDR2/3, PCI (Peripheral Component Interconnect), and USB (Universal Serial Bus) 3.0 systems, operate at rates faster than 1 Gbps. Engineers first used these links in supercomputers, communication backbones, and PCs; now, even consumer products have high-speed serial channels. Operating at gigabits per second, digital signals have entered the analog domain. A signal may never reach logic one, or it may substantially overshoot that value after traversing an IC package, a PCB (printed-circuit-board) trace on FR4 (fiberglass-reinforced 4), connectors, and cables. The signal may fall short of logic zero, or it may undershoot ground levels.

"In serial links, things like vias and via stubs become very important," notes Ken Willis, a product-marketing manager at Sigrity. "Things you don't really care about below a gigahertz make a very big difference above a gigahertz."

SERIAL-LINK PROBLEMS

Signal-integrity problems in high-speed serial links can come back to bite even the most experienced designers. You can't troubleshoot a serial channel with repetitive signals such as square waves because the signals' data pattern affects signal fidelity. You must instead stimulate the channel with a PRBS (pseudorandom binary sequence) to shake out any data-dependent problems or ISI (intersymbol interference). You then look at the resulting waveforms overlying each other to form an eye diagram (**Figure 1**).

"People who use rule-of-thumb approaches and then go right to prototype tend to be short-lived in their jobs," notes David Wiens, a business-development manager at Mentor Graphics. You need sophisticated software to simulate the channel and the companion software to extract and make simulation models of the link components (**Figure 2**). That extraction must come from the best serial-data oscilloscopes and VNAs (vector network analyzers) you can find.

Once the link is working with acceptable BERs (bit-error rates), you must ensure that the links do not interact with crosstalk, which causes new problems. When you have the entire system working, you must ensure that your system's high-speed signals don't emit too much radiation, which will cause the system to fail FCC (Federal Communications Commission) RFI (radio-frequency-interference) and EMI (electromagnetic-interference) approvals. According to Steven McKinney, a business-development manager at Mentor Graphics, 90% of companies without simulation capability must do a re-spin or use another approach to resolving their compliance problems. Omitting one board spin or preventing a late-to-market situation often pays for the entire cost of an advanced signal-integrity tool.

Evaluating the signal integrity of a serial link involves the difficult task of measuring signal integrity on a lab bench with real hardware. The channel speeds are so high that you must be careful that the probe you are using does not introduce its own loading and signal-integrity problems. In addition, the wires of the link give you an eye diagram, but that diagram is meaningless if you don't use the same equalization as the receiver chip

does to process the signal. For this task, you need sophisticated serial-data analyzers from such vendors as LeCroy, Tektronix, Agilent, and Anritsu.

Your problems continue once you begin to use software simulators. The software must model lossy transmission lines well enough for use at high speeds. Chip models must have the IBIS (input/output-buffer-information specification) AMI (algorithmic-modeling interface) to model the output driver and input receivers and the effects of equalization and pre-emphasis. The IBIS models comprise tables of time-based behavioral descriptions of a transmitting pin—similar to the way in which S (scattering) parameters comprise tables of frequency-domain behaviors of multiport systems. Executable code can represent AMI, an advanced function of the model. Thus, a chip company that has spent millions of dollars developing a sophisticated equalizer for a receiver chip or a pre-emphasizer for a transmitter can represent those algorithms in a protected, encrypted executable file that protects the intellectual property in the chip. This feature allows you to plug the model into a signal-integrity package or an advanced oscilloscope or network analyzer to learn the performance of the channel, including the equalization the chips produce.

You can easily simulate the properties of a differential pair on a lossless FR4 PCB. Unfortunately, however, signal-integrity problems require you to simulate dozens or hundreds of pairs and examine them not just for their intrinsic performance but also for the effects the channels have on each other. You may also have to model the effects of nearby power supplies or other fast digital signals. The software must solve the signal-integrity simulation using both time- and frequency-domain techniques; the tool then must apply statistical analysis to predict how jitter and crosstalk will affect the BER, EMI emissions, and RF immunity of the channel (**Figure 3**).

AT A GLANCE

- The change from parallel to serial buses emphasizes the importance of signal integrity.
- You must design high-speed serial links with specialized software.
- The channel must meet a specified bit-error rate; must not be susceptible to EMI (electromagnetic interference), RFI (radio-frequency interference), or interference with other channels; and must not radiate noise, causing your design to fail FCC (Federal Communications Commission) approval.

PRELAYOUT PROBLEMS

Signal-integrity software can help you in both the prelayout and postlayout processes, often removing risk from your product. During prelayout, the software can help you keep the channels performing to specification without radiating excessive noise. These techniques can help you make design choices, such as selecting package pinouts or connector-pin assignments, which will save you major headaches at the end of the project. When performing a prelayout analysis, you must ensure that the virtual prototype of the channel is valid and that you have accounted for expected trace lengths and board-dielectric properties. A sophisticated prelayout tool takes into account the algorithms in the chips, so you must perform a lot of experiments with any programmable settings in the virtual chips to maximize the performance of the channel.

Once you use signal-integrity software in a prelayout mode, you can delve into the board layout. You then send the layout data to the signal-integrity tools, which can predict the performance of the serial channels, the effects of the channels on neighboring circuits, and the approximate EMI radiation that your design will produce. High-end signal-integrity programs account for crosstalk between signals and the effect of power integrity on the signal.

SIGNAL-INTEGRITY SOLVERS

Signal-integrity tools act as field solvers (**Reference 1**), which use the physical configuration of a system and solve Maxwell's equations to predict the voltages and currents in the copper traces (**Figure 4**). A 3-D field solver can model the traces, wires, boards, and tin covers of a complex design, simplifying the task of using a field solver for small RF circuits and modules. A computer can often perform the huge task of solving the 3-D equations in minutes or hours. Serial channels, however, often reside on large PCBs with hundreds or even thousands of signals to account for. It would take weeks or months to solve a large board with a 3-D solver.

Signal-integrity software for 3-D field solvers makes the necessary simplifications to yield an answer in a reasonable amount of time. However, you risk an incorrect answer if you let the software use the wrong assumptions or if you do not understand the limitations of the program. You can use an inexpensive 2-D field solver to tell you the behaviors

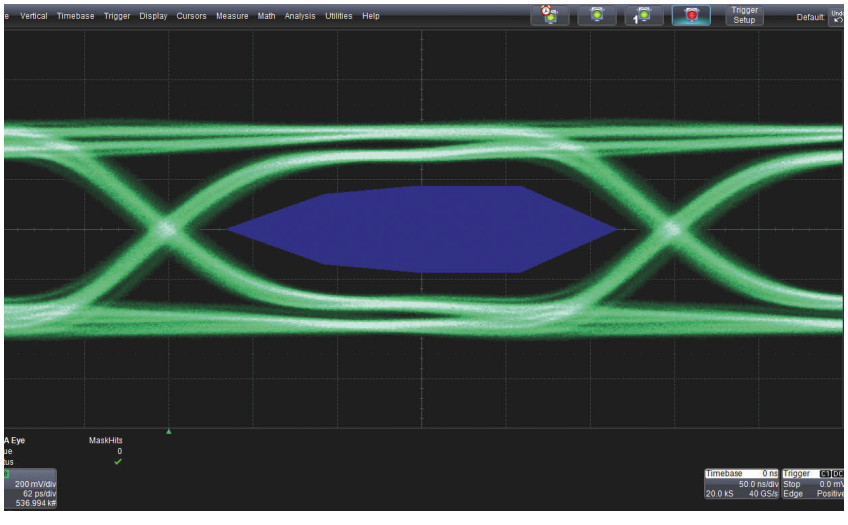

Figure 1 This eye diagram of a DisplayPort signal shows an open eye, indicating good signal integrity. Signal amplitude is self-evident, and signal jitter manifests itself as the width of the crossed portion of the superimposed waveforms (courtesy LeCroy).

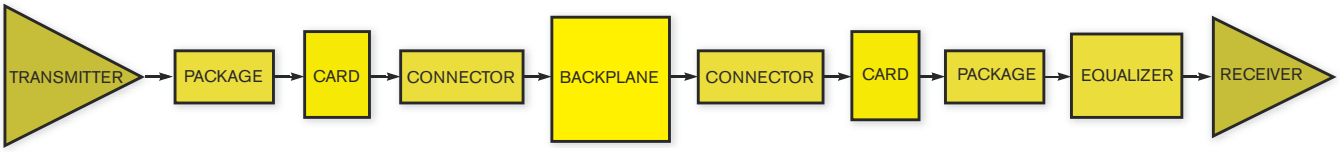

Figure 2 A high-speed serial channel comprises many blocks that you must evaluate with signal-integrity software (courtesy Sigrity).

of signals in flat PCBs. The program can model vias as capacitive discontinuities in transmission lines, a good approach for slow channels. A via has a more complex effect on a signal at speeds greater than 6 Gbps, however. At those speeds, the via is close to other copper, and its physical configuration matters, as do the layers at which the signal enters and exits. For these high-speed channels, you need a 2.5- or 3-D solver. Sophisticated tools, such as Sigrity's Channel Designer, use a 3-D solver for the vias and connectors and use 2-D techniques for traces on a plane to minimize design time.

The trade-off between computational speed and the accuracy of the result is a fundamental consideration in the selection of a signal-integrity tool. If you expect all your simulation to pertain to a 5-Gbps channel, you need software that can solve the subtle problems, including lossy dielectrics and 3-D effects, that this scenario implies. A low-power supply on the chip transmitting the serial data may also translate into poor serial-link performance. For that reason, Sigrity's Channel Designer software accounts for the effects of the channel's power system and the difference in chip performance over temperature to give you a better understanding of channel performance in real-world conditions.

You cannot feed a tool incorrect models and expect it to produce accurate results. Incorrectly modeled system blocks may exhibit passivity problems, which occur due to the component's or module's energy storage, or causality problems, which occur when you use the frequency domain to present scenarios. You can use signal-integrity software to apply an impulse function to frequency-domain models. If any aberrations or artifacts occur before the rising edge of the response, the model has causality problems, and you should investigate its validity. For this reason, models you extract with time-domain reflectometry may cause you fewer problems because they rarely yield causality problems (**Reference 2**).

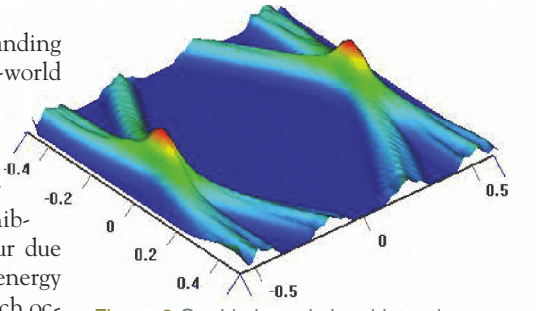

Figure 3 Sophisticated signal-integrity tools can perform analysis on the simulated data and then display it in a way that ensures the channel is working properly (courtesy Sigrity).

TOOLS

Mentor Graphics' HyperLynx is the best-known signal-integrity tool and has the biggest market share (**Figure 5**). Mentor has integrated HyperLynx into the PADS and Expedition board-layout packages, and it also works with Cadence's OrCAD and Allegro board packages, as well as those from Zuken and Altium. Altium also offers a board-layout tool that performs prelayout evaluation in the schematic editor and postlayout analysis in the PCB tool. These results tell you whether a trace has overshoot or undershoot and whether it affects a neighboring trace. In contrast, HyperLynx lets you evaluate an eye pattern and provides models of in-chip equalizers and other algorithms that plug into the tool with IBIS AMI.

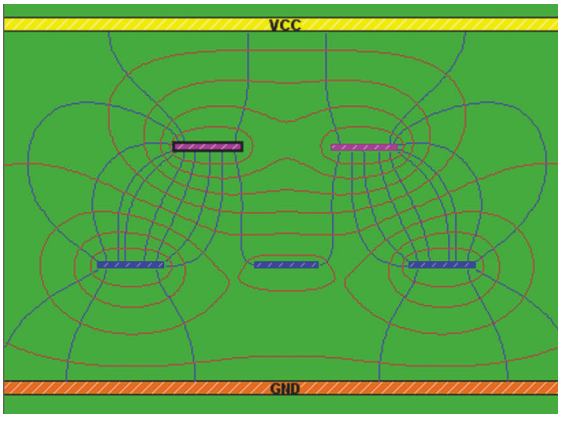

Figure 4 Field-solver software calculates Maxwell's equations and provides the voltages and currents in the traces of your PCB or system (courtesy Mentor Graphics).

According to Leslie Landers, vice president of sales and marketing at Sigrity, 10 years ago, you could only use a detailed 3-D field solver to look at a via or a bond wire or use a simulator that made simplifications that don't work in high-speed designs. Modern tools, in contrast, perform full 3-D simulation of connectors, vias, and bond wires and use faster 2-D simulation to simulate the traces on a PCB. Sigrity software can provide for the effects of the power bus on signal integrity, and other tools, including those from Sigrity and NEC, perform power-integrity analysis.

Sophisticated tools, such as those from Mentor and Sigrity, can also simulate ISI. Because the wavelength of interest is short for signals operating at 5 or 10 Gbps, you need only a few centimeters of trace length on your PCB or backplane for several of those waves to reside simultaneously on the channel. The reflections and transitions change due to the interaction of those waves. Thus, a high-end signal-integrity tool lets you excite the channel with a pseudorandom binary pattern and then collect data about the resulting eye diagram. Altium's signal-integrity tool is useful but has fewer features than HyperLynx because it is free when you purchase the $4000 Altium design platform. A fully loaded, stand-alone version of HyperLynx, on the other hand, costs almost $50,000.

Although Mentor, Cadence, Zuken, and Altium have used their experience in board design to develop signal-integrity tools, you can also obtain good tools from other sources. Several companies make field solvers and signal-integrity tools. Ansoft, second only to Mentor in market share, uses its expertise in mathematical computation and plotting to help engineers solve signal-integrity problems. Ansoft's flagship product, HFSS (high-frequency structural simulator), is a general-purpose field solver that also allows Spice modeling for S parameters and matrix solvers. Ansoft's DesignerSI software includes schematic-capture and layout tools, a 2-D field solver, and the statistical and IBIS capabilities needed to design a serial link (**Figure 6**). Ansoft also offers SIwave to extract models from board and package geometry.

SiSoft, an early champion of the IBIS AMI standard, offers the Quantum-SI field solver, which performs both prelayout and postlayout signal-integrity analysis. SiSoft also offers the Quantum Channel design environment for high-speed serial links. SiSoft's tools model algorithms and equalizations in transmitter and receiver chips and perform automated compliance testing to tell you whether your channel will comply with a given interface standard, such as PCIx (Peripheral Component Interconnect Extended) or IEEE 802.3xx. The program interfaces with several board programs, including Mentor's Expedition PCB and programs from Allegro, Altium, and Zuken. Many field-solver programs, including those from Comsol, Sonnet Software, CST, and E-System Design, also handle calculations for signal integrity. Most large field-solver companies offer 3-D programs that accurately model connectors and bond wires. Modeling a large PCB in 3-D is often time-consuming, however.

Because signal-integrity problems manifest themselves at high frequencies, RF-design-tool companies have stepped up to help engineers with signal integrity. Agilent, for example, offers both the EMDS (electromagnetic-design-system) and the ADS (advanced-design-system) field solvers. ADS comes with signal-integrity plug-ins that let you visualize fields and currents in 3-D. Agilent also recently added support for IBIS AMI models. AWR's Microwave Office, meanwhile, touts ease of use and an intuitive interface; the company also offers signal-integrity tools, such as the SI Design Suite, which can help with 2- and 3-D analysis.

"Many companies are asking their RF engineers to help with signal-integrity and EMI issues," says Sherry Hess, vice president of marketing at AWR. "It is

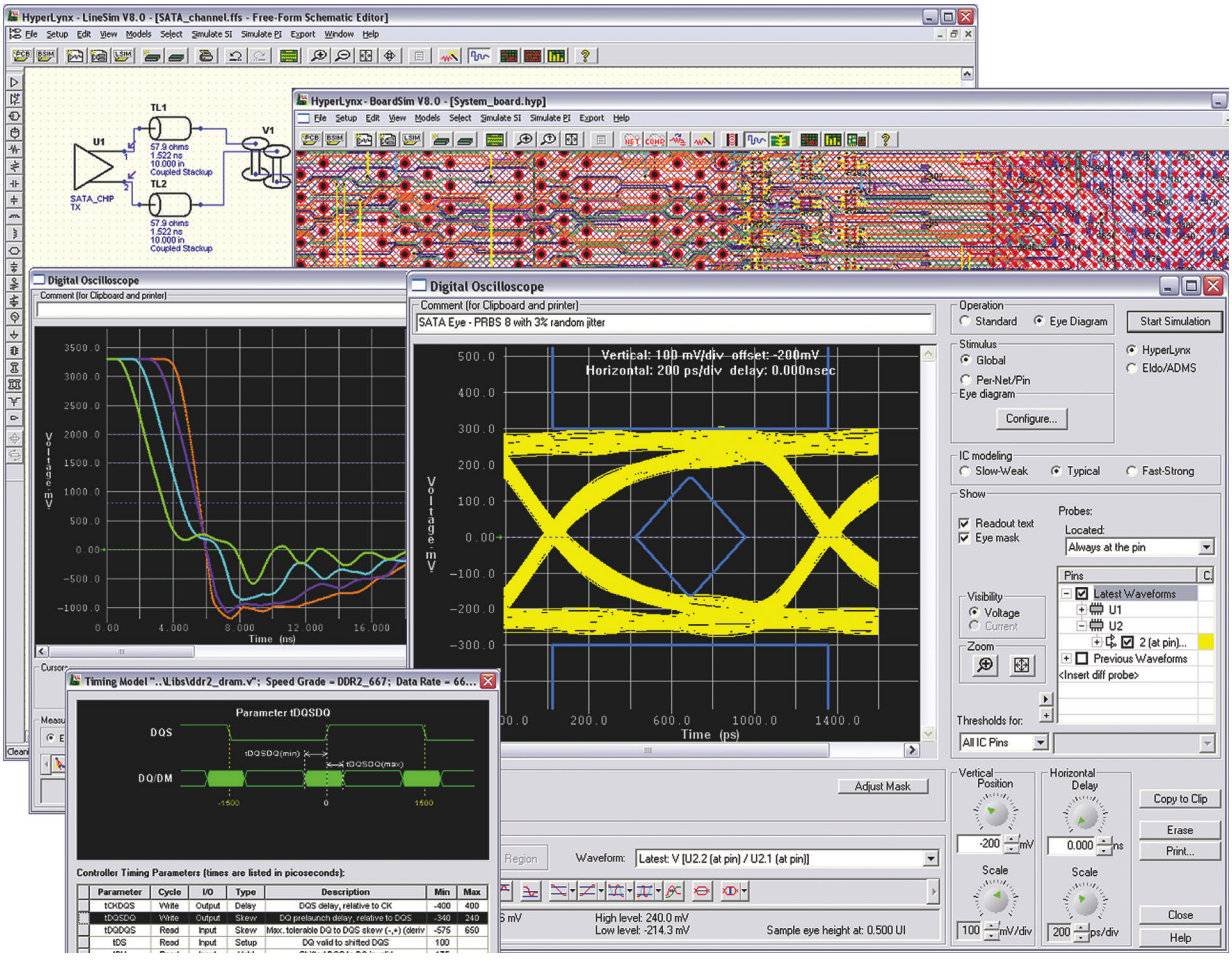

Figure 5 Mentor Graphics' HyperLynx is the best-known and most popular signal-integrity tool.

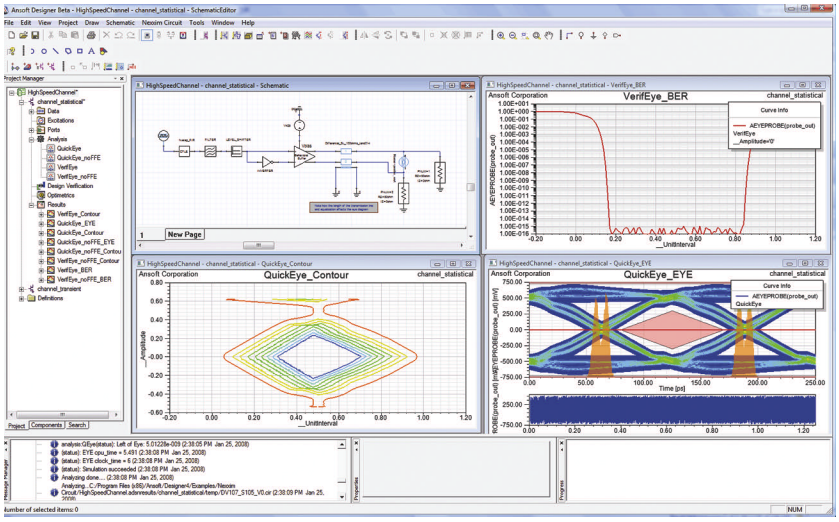

Figure 6 Ansoft offers its own fully featured signal-integrity tool for high-speed-serial-channel design.

only natural that those engineers prefer to use the RF-design environments they are used to."

Joining board-layout-, field-solver-, and RF-tool vendors, mathematical-analysis companies, including The MathWorks, can also help with serial-channel signal-integrity problems with tools such as Matlab. Matlab's toolboxes include series of application-specific mathematical functions, according to Giovanni Mancini, marketing manager for RF and analog products at the company. Tools such as ADS and Microwave Office generate simulations of lumped-element models, and Matlab uses those models to analyze the channel model. You can use the statistical capabilities of Matlab to predict BER. Matlab is also useful in developing the filter algorithms for the equalization functions in the receiver chips.

"Engineers use Matlab at different stages of the design and characterization phase," says Chris Aeden, manager of the marketing group for signal processing and communications at The MathWorks. "The communications toolbox allows engineers to enter and test data waveforms to evaluate those filters."

Chip companies can also help designers address signal-integrity problems. "We provide tools so that you can do analysis before finishing the layout and tools for after you do the layout," says Oliver Tan, a senior product-planning engineer at Altera. One such tool, the SSN (simultaneous-switching-noise) estimator, works during prelayout to model the SSN that inductive crosstalk generates.

The SSN-analyzer tool works during postlayout to help you evaluate signal integrity and choose the FPGA's pinouts. "Even low-end products are using 1 to 3-Gbps links," says Phil Simpson, senior manager of technical marketing at the company. "The problem changes significantly as you get to higher data rates."

Mentor Graphics, Zuken, and Cadence point out that their signal-integrity tools work within their PCB-design flows. Remember, however, that those integrated tools often started out as separate or point tools that these companies purchased and then integrated into their flows. "A function is not truly integrated unless the entire flow works off the same database," says Gerry Gaffney, regional chief executive officer at Altium. Hence, it is important to select the signal-integrity tool that best serves your needs.

Sigrity's Willis notes that the company doesn't want to compete with PCB tools such as Expedition and Allegro but ensures that Channel Designer works well with those and other PCB tools. He contends that the availability of a point tool allows the company to concentrate on signal-integrity problems, as the advanced performance of Sigrity's software demonstrates.

A signal-integrity tool must use an entire arsenal of techniques to keep the sharks at bay. The tools for high-speed channels must perform both 2- and 3-D field solving, as well as matrix computations with Spice. The tools must also evaluate time-domain performance employing the S parameters of the modules in the channel and provide data-analysis capability to help you infer the BER from a given jitter or crosstalk simulation. "A lot of designers aren't educated in signal integrity at all," says Altera's Simpson. "They need tools to tell them whether the design will work." Achieving that goal demands the best software you can get. **EDN**

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BY PAUL MAGILL, PhD • NEXTREME THERMAL SOLUTIONS INC

Active heat removal cools electronics hot spots

A NEW APPROACH TO THERMAL MANAGEMENT INVOLVES EMBEDDING FUNCTIONS DEEP INSIDE AN ELECTRONIC COMPONENT AT THE SOURCE OF THE HEAT USING THERMOELECTRIC DEVICES.

Electronic components, packages, and systems continue to shrink even as they gain more functions. These dense electronic systems generate a lot of heat that can lead to a significant rise in temperatures, causing device and system-level failures. You can use active or passive cooling techniques to solve these problems. TECs (thermoelectric coolers) are active systems; passive systems include thermal-interface materials, heat spreaders, and heat sinks.

To understand the design challenges facing engineers in the electronics industry, you first must consider the way heat flows through a material system and the forces that govern that movement. Heat has long been an issue for system designers, but the problem has recently become severe. Designers must view thermal management not as an afterthought but as an issue they must deal with from the beginning of the design process. Heat's continuous flow from one material to another creates a temperature gradient across those materials.

Designing a thermal-management system today requires designers to view the means for moving the heat and the manner and location in which the design rejects the heat early in the design cycle to avoid causing severe problems at the system level. This consideration is important because the thermal operating range—that is, the temperatures the system can tolerate—is more limited, and any approach you employ at the system level is likely to be more expensive than one you implement at the chip level.

Unfortunately, the management of heat in a system is at times somewhat like pushing jelly. You can press it down in one direction, but doing so causes it to flow in another. To see why this situation occurs, you can look at the rules for heat flow in a material system. After acquiring a basic understanding of the rules, you can apply them to both passive and active devices.

HEAT FLOW

The heat equation is an important partial differential equation describing the distribution of heat, or variation in temperature, in a given region over time. For a function u(x,y,z,t), which is a measurement of the temperature, T, of three spatial variables—x, y, and z—and the time variable, t, the heat equation is:

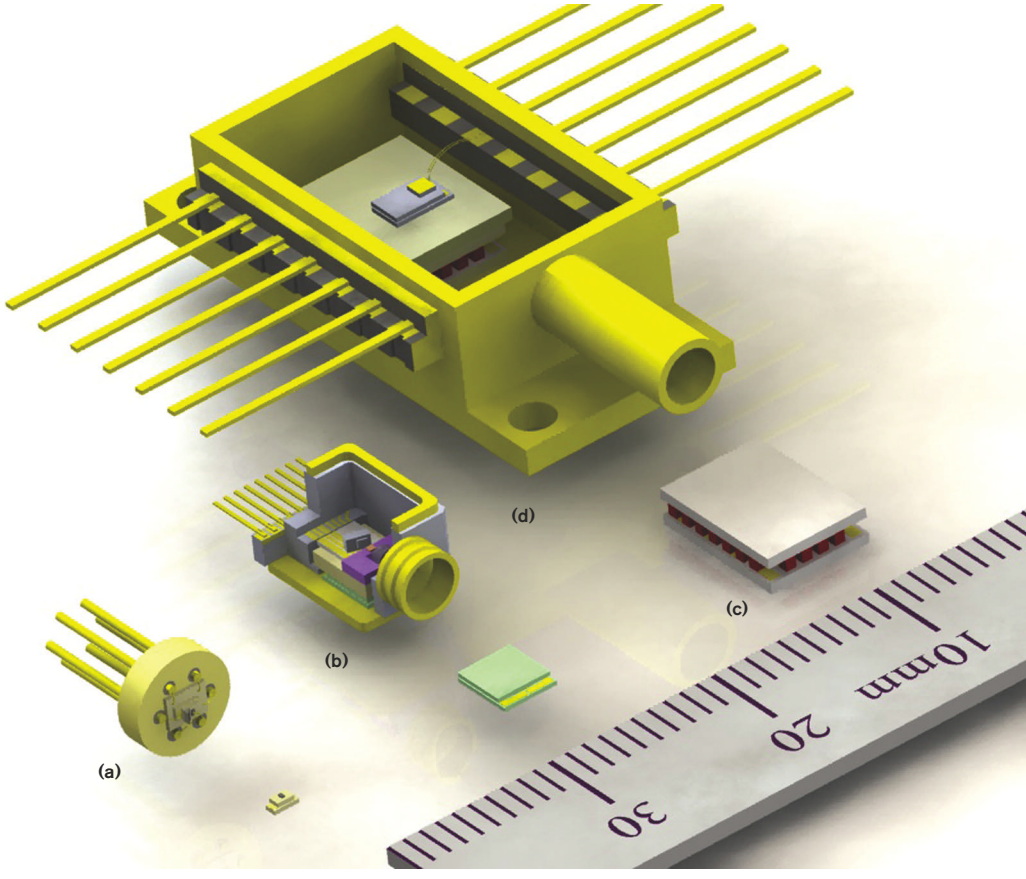

Figure 1 Optoelectronic packages, including the butterfly package (a), the TOSA-style package (b), and the TO-56 package (c), continue to get smaller, as do TECs (d).

$$\frac{\partial u}{\partial t} - k\left(\frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} + \frac{\partial^2 u}{\partial z^2}\right) = 0,$$

where k is the thermal diffusivity of material. Equivalently,

$$\frac{\partial u}{\partial t} = k\nabla^2 u,$$

where k is a constant.

The other important governing equation is Q=U+W, where Q is heat flow, U is the change in the internal energy of the system, and W is work on the system. That is, heat flow is equal to the work on the system plus the change in internal energy of the system. Hence, the change in heat is equivalent to the heat flowing into the system. Combining these two equations, and in the absence of any work, Q is proportional to the change in temperature. Thus, you arrive at Q=ΔT, where ΔT is the change in temperature. For passive systems, cooling by the conduction of heat is a linear function of temperature and a constant related to the material properties of the solid. This constant, k, may be a function of many variables, including temperature, power, and voltage.

The primary systems for passive cooling of electronic and optoelectronic systems are thermal-interface materials, heat spreaders, and heat sinks. Each performs a different function for removing heat from a system. Heat sinks may be an environment, such as water or air, or an object that absorbs and then dissipates heat while in physical or thermal contact. This dissipation may occur through direct or radiant transfer of heat. Heat-sink performance is a function of material, geometry, and the overall surface-heat-transfer coefficient along with the temperature of the heat sink. Generally, you can improve forced-convection heat-sink thermal performance by increasing the thermal conductivity of the heat-sink materials and increasing the surface area.

Thermal-interface material fills the gaps between thermal-transfer surfaces, such as microprocessors and heat sinks, to increase thermal-transfer efficiency. Air, a poor conductor, normally fills these gaps. The most common thermal-interface material is white paste or thermal grease—typically, silicone oil encapsulating aluminum oxide, zinc oxide, or boron nitride. Heat spreaders are most often simply metal plates having high thermal conductivity. Designers also use carbon-based heat spreaders with anisotropic characteristics. They act as heat exchangers, moving heat between localized heat and a secondary, larger heat exchanger. Heat moves through all these passive components only with a temperature difference from a higher to a lower temperature. The rate of flow is proportional to the difference in temperature. Both active and passive approaches can cause or assist in this flow.

THERMOELECTRIC COOLING

If you want to continue to shrink your devices, you must also shrink the thermal-management system. Because passive heat removal is only a linear function over distance of the temperature difference, you must put work into your system to obtain a greater rate of cooling and hence a smaller device. **Figure 1** shows one example for optoelectronics of the continuing reduction in device size. In some instances, designers place the cooling device outside the package if it is too large to fit inside.

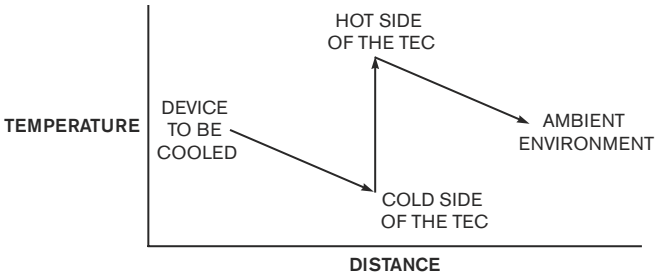

Figure 2 TECs provide heat pumping and temperature control.

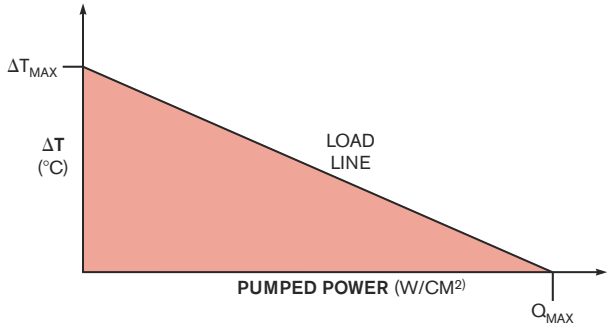

Figure 3 The load line represents the change in temperature and pumped-power conditions possible for a TEC's drive current and defines the operational space for TECs.

A TEC is an active thermal-management device that can provide additional heat pumping and temperature stabilization. **Figure 2** shows a simple example of the type of heat pumping and temperature control you can get from a TEC. TECs use the Peltier effect to create a heat flux between the junctions of two types of materials. Peltier coolers, heaters, and thermoelectric heat pumps are solid-state active devices that transfer heat from one side of a device to the other side against the temperature gradient—from cold to hot—as they consume electrical energy. People also refer to devices that operate in this manner as Peltier devices, Peltier diodes, Peltier heat pumps, solid-state refrigerators, or TECs.

The most basic representation of the operational space for a thermoelectric cooling device is a load line (**Figure 3**). The load line represents the ΔT and Q_{PUMPED} (heat-removed) conditions possible for a TEC's drive current. At the maximum drive current for the module, the maximum power the device can pump, Q_{MAX}, and the maximum temperature difference that the device can sustain between its top and bottom plates, ΔT_{MAX}, generate the load line. The ΔT_{MAX} condition occurs when the device reaches a zero-Q condition—that is, when no heat is flowing through it. You can theoretically calculate the value with the following **equation**:

$$\nabla T_{MAX} = \frac{\alpha^2 T_C^2}{2k\rho} = \frac{\alpha^2 T_C^2}{2KR},$$

where α is the Seebeck coefficient, k is the thermal conduc-

tivity, ρ is the electrical resistivity, T_C is the cold-junction temperature, K is the thermal conductance, and R is the resistance.

The Q_{MAX} condition occurs when there is no temperature difference between the top and the bottom of the TEC:

$$Q_{MAX} = \frac{A\alpha^2 T_C^2}{2\rho L} = \frac{\alpha^2 T_C^2}{2R},$$

where A is the area of the device and L is the length, or thickness, of the thermoelectric material. You can graph the two parameters on a chart as ΔT_{MAX} at $Q=0$; Q_{MAX} at $\Delta T=0$. The line connecting them is a load line. The resulting load line defines the operational space for TECs and is the best and usual way to illustrate their performance.

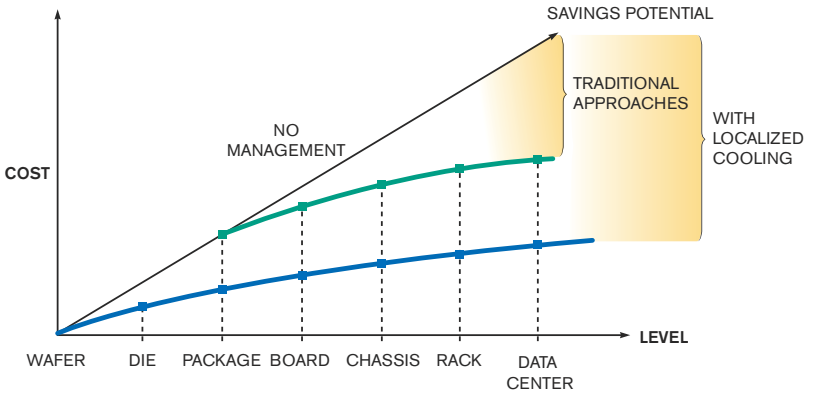

Figure 4 Localized cooling in a data center can be more efficient than removing heat from the servers to the server room and then cooling the entire room with air conditioning.

With the exception of fans, which usually work in conjunction with heat sinks, most of today's thermal-management systems are passive types. Conduction-based thermal-management systems, such as thermal-interface materials, improve the flow of heat from one location to another, greatly enhancing the efficiency of the overall thermal-management system. However, convection-based systems have the drawback of allowing heat to flow in an uncontrolled manner from one level to the next. These systems have served the industry well but have the drawback of removing not only the heat that is limiting device performance but also any of the heat from the surrounding area, which likely is not limiting the device or system performance.

One approach to this problem is to use an active device inside the electronic package for localized thermal management. To reduce the cooling necessary at the system and building levels, however, you must reduce the amount of heat you extract from the die. Cooling the die generally keeps their operating frequency near its peak. However, the temperature within one of the hot spots on the die and not the temperature across the entire die typically limits this peak frequency. Instead of extracting the heat from the die as a whole, you could extract the heat only from the hot spot. In this way, you are dealing with a smaller system-level problem and subsequently have a smaller thermal-management problem.

TEC-DESIGN ISSUES

One of the drawbacks of TECs is that they consume power while performing the task of cooling. This power adds to whatever power the cooling zone is pumping out, so the system dissipates more heat at the larger system level with a TEC in operation than without one. If you use TECs to cool devices in the same manner as passive thermal elements—in other words, everywhere—you will end with a larger problem at the system level than you just solved at the chip level. A more cost-effective and efficient approach—and one that is possible only with TECs—would be to cool only what is necessary. In other words, scale the thermal-management system to the size of the heat problem.

The following **equation** illustrates the coefficient of performance of a TEC:

$$COP = \frac{Q_{PUMPED}}{P_{IN}},$$

where COP is the coefficient of performance and P_{IN} is the input power.

A TEC pumps a certain amount of heat, Q, and adds a particular amount of heat, Q×COP, to move this heat. This situation results from the inherent inefficiency in all engines. As a result, vendors of bulk TECs often sell them as systems that include the device itself and a heat-transfer device, such as a fan, heat sink, or heat pipe. The value of the TEC in this case is that it can deliver subambient temperatures and provide active temperature control, but at the cost of increasing the system-level heat-transfer problem.

Because heat in the passive case flows linearly, any material between the TEC and the heat source has a temperature drop across it. This decrease increases the temperature difference that the TEC must pull. The TEC acts as a heat pump moving heat in a manner whose efficiency depends upon the temperature difference it must generate. Minimizing this temperature difference improves the efficiency of the cooler and reduces the additional heat at the system level.

Integrating a TEC close to the heat source is the key to improving the TEC's operational efficiency. Adding a heat-transfer system defeats the purpose of the integration. As such, you must pay careful attention to the characteristics of the heat-transfer problem, the design of the TEC, and the design of its package. When you address these issues—ideally during product design and development—you can achieve significant performance improvements.

LOCALIZED THERMAL MANAGEMENT

Dense electronic systems generate a lot of heat that can lead to a significant rise in temperatures, causing device and system-level failures. The answer to these problems has always been to use a larger fan or a larger heat sink to move the heat from the electronic package and into the system environment. However, the use of fans and heat sinks merely spreads the heat into other systems, such as enclosed equipment racks, which then require a thermal-management approach of their own. Heat from these racks usually spills into the system room or IT data

center. These rooms, with people working in them, are sensitive to high temperatures. Tackling this problem requires the use of expensive air conditioners, which cool everything in the room to the lowest possible temperature.

The Environmental Protection Agency (www.epa.gov) projects that US data centers will consume more than 100 billion kilowatt-hours by 2011, representing an annual cost of at least $7.4 billion. According to a recent study by Emerson Network Power (www.emerson.com), 50% of the power that data centers consume goes toward air conditioning for battling heat. As this cascading method of heat rejection moves from the local scale to the more global scale, thermal-management systems use more electrical power to manage this heat rejection and therefore become more costly.

The most efficient thermal-management system involves embedding thermal-management functions at the source of the heat to remove only the heat that is detrimental to the system's performance and then passing on that reduced heat in a controlled manner to the next level. **Figure 4** compares the cost of implementing thermal management with the level at which the technique occurs. Implementing heat sinks, fans, and large-scale cooling creates an energy-savings potential. Introducing localized cooling in the overall thermal-management design translates to a greater cost-savings potential at the rack and data-center levels.

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Today's electronic systems typically employ only passive elements for thermal management. This approach removes heat uniformly from across the die. The point of heat removal, however, is to reduce the peak temperature on the die to improve performance. The heat associated with the peak temperatures on a die is only a small fraction of the total removed heat. Removing this excess heat leads to problems at the system and eventually the building levels, as the example of thermal management in data centers illustrates.

Solving the thermal-management issues at the die, system, and building levels requires a paradigm shift. Integrating localized thermal management that combines active and passive components within electronic systems allows you to flatten the power map on a die and minimize the waste your system must dispose of. This type of selective removal of heat simplifies issues at the system level and reduces cost. EDN

AUTHOR'S BIOGRAPHY

Paul Magill, PhD, is vice president of marketing and business development at Nextreme Thermal Solutions Inc and has more than 20 years of experience in the electronics and optoelectronics industry, with expertise in sensors and laser-diode applications as well as electronics and MEMS (microelectromechanical-system) packaging and manufacturing. He holds both bachelor's and master's degrees in physics from the University of North Carolina—Charlotte.

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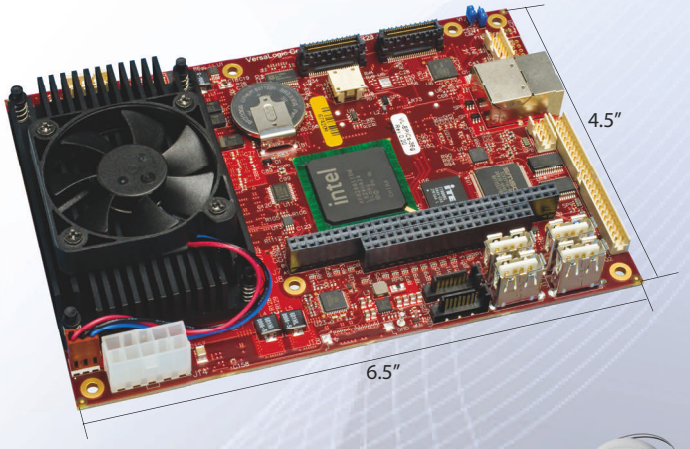

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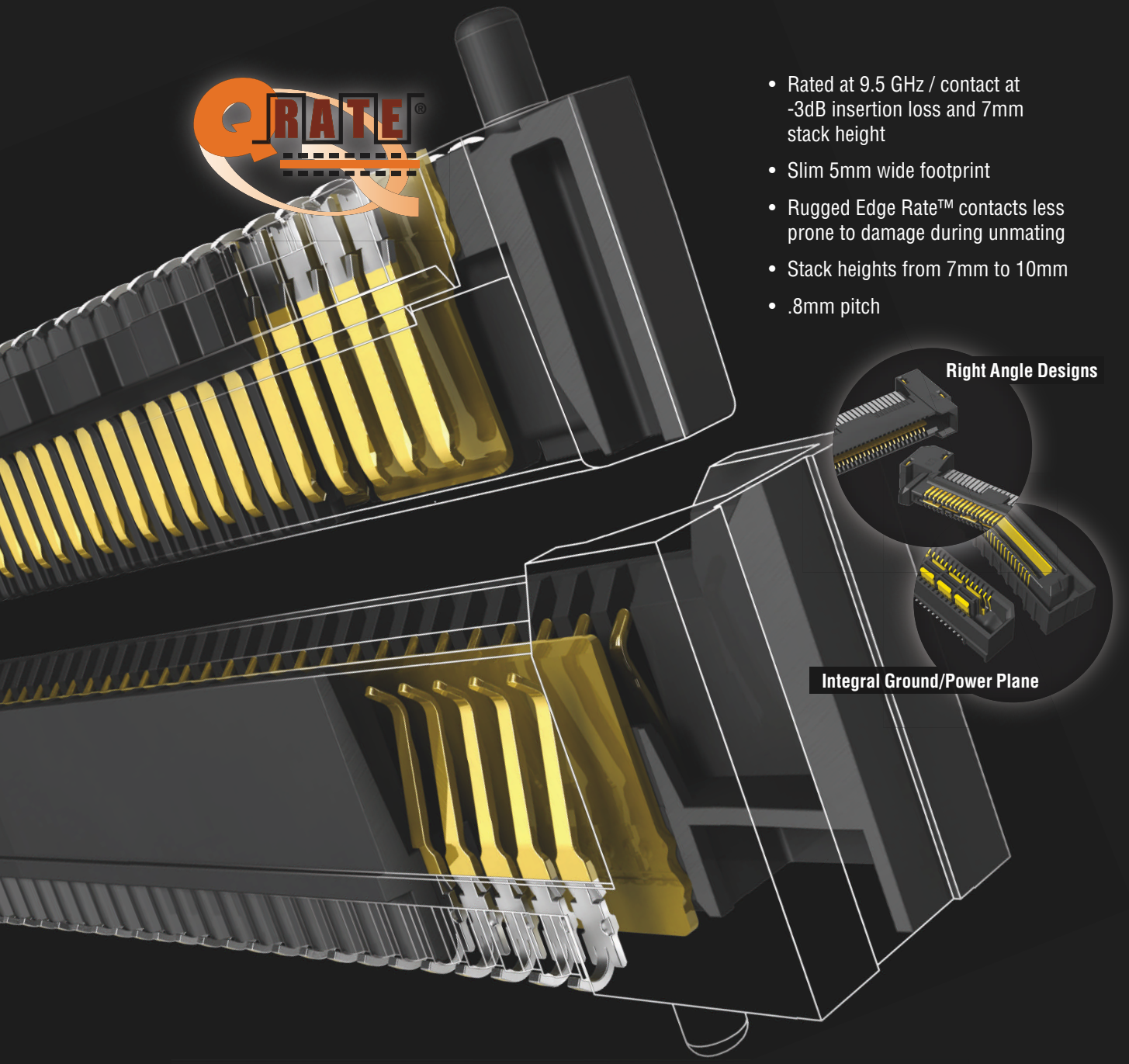

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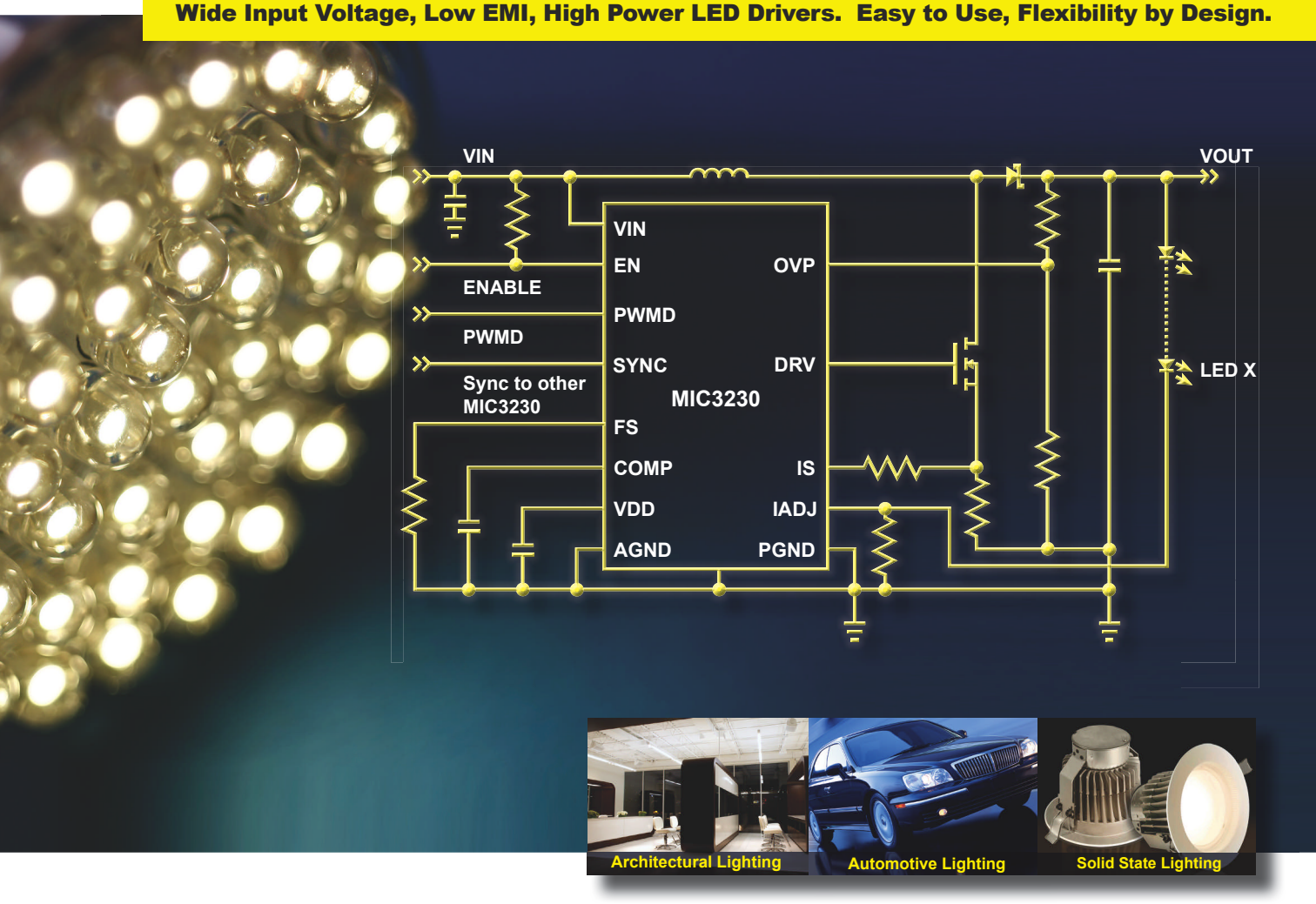

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BY CALVIN DU • MEDX HEALTH CORP

Integrating midsized LCDs

WHEN INTEGRATING LCDs INTO YOUR DESIGN, YOU NEED TO CONSIDER NOT ONLY THE COST OF THE LCD ITSELF BUT ALSO THE COSTS OF RELATED HARDWARE, SOFTWARE DEVELOPMENT, RTOS, AND MECHANICAL COMPONENTS.

With the growing demand of better user interfaces in compact commercial, industrial, and medical applications, midsized, 4- to 10-in. QVGAs (quarter-video-graphics arrays) and VGAs are replacing the traditional character or small graphics LCDs. However, this type of application usually uses microcontrollers, entry-level microprocessors, or DSPs, and the integration of LCDs requires both hardware upgrades and software efforts. Several common ways are available for driving midsized LCDs, and designers must compare the topology, hardware, and software requirements, as well as the costs of these approaches, especially for microcontroller-based systems.

A typical design for driving an LCD includes a CPU, the RAM, the LCD controller, drivers, and the LCD panel itself (**Figure 1**). The LCD comprises a number of pixels arranged in a matrix. In the LCD buffer, each pixel has a piece of corresponding data ranging from 1 bit to a few bytes, which controls whether the pixel is on or off, as well as its color or gray scale. The driver shifts and latches the data into row and column registers that directly drive the LCD at the lowest level, so the drivers are also known as the row and column drivers. The LCD controller, which functions above the level of the drivers, is in charge of receiving data and instructions from the CPU, updating the display buffer, and sending the display data to the drivers following the rigorous timing requirements that the LCD and drivers specify. The CPU does all the high-level functions, such as drawing characters or images, to provide the graphics interface for the application.

The common interfaces for small LCDs are the Motorola (www.motorola.com) 6800 and Intel (www.intel.com) 8080 CPUs because these units ease the integration of the LCD controller and drivers into the module. When the LCD resolution in the system is more than approximately 320×240 pixels, the system needs more RAM, more drivers, and a higher-performance controller. For a midsized LCD, the common practice is to build only the drivers within the LCM (liquid-crystal-display module) and use an external, separate LCD controller. You can also build the LCD controller into the LCM or the CPU. Depending on the variations of the design, each design topology requires different hardware and software efforts to achieve the same goal.

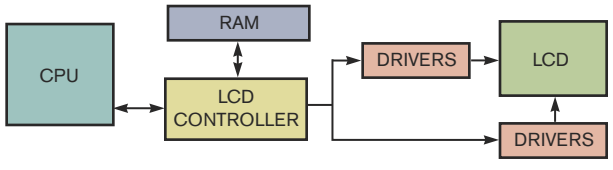

Figure 1 A typical design for driving an LCD includes a CPU, the RAM, the LCD controller, drivers, and the LCD panel itself.

TOPOLOGIES

An external LCD-controller topology, comprising a CPU with an LCD controller and an LCM, is the most popular and straightforward configuration for driving the LCD. All of the main components are standard and widely available. The CPU can be a microcontroller, a microprocessor, a DSP, or an SOC (system on chip). Most complex system designs use microprocessors, whereas microcontrollers and SOCs are more appropriate for the compact and portable designs because of their lower costs.

Not all CPUs can connect to an LCD controller. The basic requirements are the address and data bus and related controls. This is not a problem for microprocessors and DSPs, but some microcontrollers lack these features. Some microcontroller vendors provide an LCD interface to enable the microcontroller to smoothly connect to an LCD controller. A few examples are the ST32F10 family from STMicroelectronics (www.st.com), the LPC2888 family from NXP (www.nxp.com), and the PIC24F family from Microchip (www.microchip.com).

A CPU with a built-in LCD-controller topology comprises a CPU and an LCM (**Figure 2**). There is a difference between the drivers and the controller, especially in comparing microcontrollers with built-in LCD controllers versus those with column/segment drivers, which mainly target applications with small LCDs.

Many microprocessor and DSP families are on the market, but the challenge is to select one with reasonable cost to fulfill your application's requirements. Only a handful of microcontrollers are available, but more are becoming available, some of which fit well into compact or portable designs. These devices include the Bluestreak series, which NXP in 2007 purchased from Sharp (www.sharp.com), the LPC2478/2470 family from NXP, the MCF5227x family from Freescale (www.freescale.com), and the AT91CAP family from Atmel (www.atmel.com).

Another topology comprises a CPU that directly connects to an LCM with a built-in LCD controller (**Figure 3**). The module interface usually supports the Motorola 6800 bus, the Intel 8080 bus, or both. This topology prevails in small-graphics-LCD applications with resolutions of 128×64 dots or less. In these applications, the LCM integrates the LCD controller, the drivers, and the RAM. For midsized-LCD applications, this topology largely reduces the design and development time

and, hence, the time to market. However, this topology costs more and makes it more difficult to find an alternative part and integrate it into other similar production lines.

An interesting topology comprises a CPU that directly connects to the LCM without an LCD controller (**Figure 4**). By using the parallel interface and the DMA (direct-memory-access) engine, the system can perform the function of the LCD controller. This approach costs less in hardware for the application with an LCM comprising a midsized LCD, but it requires a greater software-development effort. The CPU uses the DMA to continuously move the data in the display buffer to the LCM with the help of the timers and other special-function blocks. A few examples are the H8S/H8SX microcontroller from Renesas (www.renesas.com), the BF51x Blackfin DSP from Analog Devices (www.analog.com), and the S12X family from Freescale. For designs with an LCD controller, you can use an FPGA with an IP (intellectual-property) core to replace the LCD controller. If the system includes an FPGA, it is probably a good idea to upgrade it to include the IP-core LCD controller.

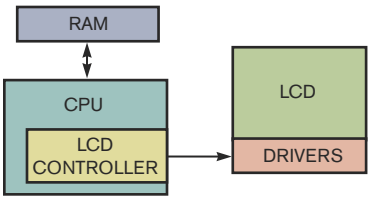

Figure 2 A CPU with a built-in LCD-controller topology comprises a CPU and an LCM.

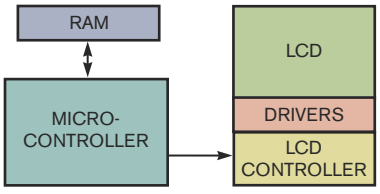

Figure 3 Another topology comprises a CPU that directly connects to an LCM with a built-in LCD controller.

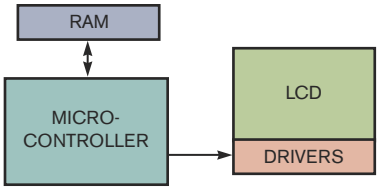

Figure 4 An interesting topology comprises a CPU that directly connects to the LCM without an LCD controller.

SPECIFICATIONS

With the topology in mind, you need to carefully consider specifications such as size, technology, interface, backlighting, brightness, and resolution. Keep in mind that the active area of an LCD consists of all dots, and the viewing area consists of the active area plus the edge. The outline size is the mechanical size of the LCD.

The size of the LCD dictates the use of different technologies. Midsized LCDs typically use TFT (thin-film-transistor), STN (supertwisted-nematic), FSTN (fast-STN), CSTN (color-STN), and OLED (organic-light-emitting-diode) technologies. TFT LCDs generally have higher quality than the STN LCDs and are better for color displays, even though lower-cost CSTN LCDs have a large share of the market. OLED LCDs are just emerging for use in small displays and are now beginning to support midsized LCDs, as well.

Monochrome LCDs, which are available in black and white, blue, green, gray scale, and other colors, are good choices for low-cost systems. Using these devices eliminates not only their cost but also the cost of the associated hardware resources and software efforts. STN LCDs dominate this area, although they are facing a challenge from OLED LCDs.

Different LCDs require different levels of system resources, including RAM, bus frequency, and CPU performance. Consider, for example, the display data for a single frame in a 320×240-pixel LCD (**Table 1**). Displaying more data in a frame requires a faster clock and a higher-performance CPU.

The most common interface for use with these LCDs is a 4- to 18-bit parallel interface. Black-and-white STN and FSTN LCDs typically use 4- or 8-bit interfaces; CSTN LCDs typically use 8-, 12-, or 16-bit interfaces; and TFT LCDs typically use 18-bit interfaces. LCMs with built-in controllers use digital interfaces—the data bus, the address bus, and the control bus. Advanced LCMs that include a microcontroller may use a serial interface, such as a UART (universal asynchronous receiver/transmitter), an I^2C (inter-integrated circuit), or an SPI (serial-peripheral interface).

LEDs and CCFLs (cold-cathode-fluorescent lamps) are the two main technologies for backlighting. LED is the newest technology, so not all LCMs have LED backlights. CCFL backlights need special inverters, and LED backlights need LED drivers, which provide constant current to the LEDs. Another type of backlighting, electroluminescent, needs a special driver to generate the required high voltage.

Brightness is another key feature to consider, especially for outdoor applications. Some ambient-light sensors help with dynamically changing the backlight to save energy without losing the display quantity. These LCDs typically have 320×240- or 640×480-pixel resolutions. The higher resolution the LCD has in the same size, the better the display quality will be.

In addition to these specifications, a designer should find two or more compatible LCDs as backups in case one of them disappears when you start or are in the middle of production. Having an alternative part available is important, especially for medical applications, which usually have a longer production life. Changing the LCD in the system usually causes mechanical, electrical, and software changes, as well.

TABLE 1 DISPLAY DATA FOR ONE FRAME

Type	**RAM size** (kbytes)	**Sample data** (2 bytes)
TFT (16 bits/pixel)	320×240×2=153.6	RRRRRGGG GGGBBBBB=1 pixel
CSTN (3 bits/pixel)	320×240×3/8=28.8	RGBRGBRG BRGBRGBR=5⅓ pixels
Black and white (1 bit/pixel)	320×240×1/8=9.6	DDDDDDDD DDDDDDDD=16 pixels

HARDWARE INTERFACE

Dedicated LCD controllers generate the

required signals. In designs without LCD controllers, however, the CPU generates the required signals. The main signals of a typical color TFT LCM without a built-in LCD controller include the data signal, the data-clock signal, the horizontal-synchronizing signal, the vertical-synchronizing signal, and the enable signal. Almost all LCMs for midsized LCDs use an 18-bit data signal in the format of R(0..6), G(0..6), B(0..6). Because the CPU's port is 16 bits wide, LCDs often use the RGB (red/green/blue)-565 color mode, which has 5 bits per color, plus an extra bit for green because the green component contributes most to the brightness of a color in the human eye.

IN ADDITION TO THE LCD COST, CONSIDER THE COST OF RELATED HARDWARE, SOFTWARE DEVELOPMENT, RTOS, AND MECHANICAL PARTS.

During the data-clock signal, each cycle shifts the 16 bits of RGB data of one pixel. For each line, the clock number is equivalent to the column number of the LCM. The horizontal-synchronizing signal specifies when to start a new line, and the vertical-synchronizing signal specifies when to start a new frame. The horizontal-synchronizing pulse has three important timing characteristics: the "front porch," the pulse width, and the "back porch." The front porch of the synchronizing pulse is the delay between the end of the video data of a scan line and the initial edge of the synchronous pulse. The pulse width is simply the period of time that the synchronous signal is asserted, and the back porch is the delay between the final edge of the synchronous pulse and the first piece of data for the next scan line. The enable signal is optional and represents the period during which data shifts. When using automatic continuous clocking without this signal, you must add the front and back porches to sandwich the data of each line, and you must add extra lines before and after each frame.

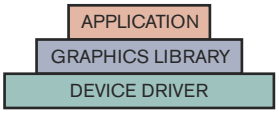

Figure 5 The three base layers of software are the device driver, the graphics library, and the application layer.

The main signals of a typical monochrome STN LCM are similar to those for the TFT LCM. The data signal is in the format of D(0..3). During the data-clock signal, each cycle shifts 4 bits of data, which represent 4 pixels. So the clock number of each line equals one-fourth the column number of the LCM. The second clock signal specifies when to start a new line, and another signal specifies when to start a new frame. In a typical color STN LCM, the data signal is in the format D(0..7). During the data-clock signal, each cycle shifts 8 bits of data, in which every 3 bits represent a pixel. The clock number of each line equals N×3/8, where N is the column number of the LCM. A second clock signal specifies when to start a new line, and the first-line-marker signal specifies when to start a new frame.

SOFTWARE DEVELOPMENT

You can develop the embedded software of compact systems with or without an RTOS. Because these systems' LCD-based user interfaces are more complicated, designers are increasingly developing this type of embedded software on a commercial or free open-source RTOS. Regardless of whether you use an RTOS, however, the principal function of the code is the same. The three base layers are the device driver, the graphics library, and the application (**Figure 5**). The device driver configures the registers related to low-level communication with the LCD controller, such as DMA, the parallel port, and the display buffer; all of these units are highly dependent on hardware. The driver provides a standard set of graphics-related fundamental functions no matter how different the hardware is, which makes the layers above the device driver easier to port from one design to another, saving time and money. This layer, although usually just a small piece of code, is important.

The layer above the device driver is the graphics library. It includes functions to draw a pixel and a line, generate the characters, and draw an image. It also includes advanced functions to create a modern interface, such as buttons, check boxes, and edit boxes. Systems with an RTOS come with a graphics library. For those without an RTOS, you can either write a library yourself or buy a package from a third party. The highest and the last layer is the main application of the design.

For a system without an LCD controller, the CPU directly connects to the LCM. The software must generate all the timings and clock the data into the LCM. So the software device driver must do a lot of work. A handful of CPUs, including the Blackfin DSP, support this approach. The Blackfin can drive both monochrome STN/FSTN and color TFT displays. It uses the PPI (parallel peripheral interface) and DMA to transfer the pixel data directly to the LCM, and it uses timers to generate the PPI clock, the horizontal-synchronizing signal, and the vertical-synchronizing signal. It also uses GPIO (general-purpose input/outputs) to implement other controls. When writing the code for the device-driver layer, the main tasks include configuring the PPI, DMA, timers, and GPIO registers and allocating the display buffer. You can use an emulator and an oscilloscope to verify that the code generates the expected signals.

In summary, when designing an application with a midsized LCD, in addition to the LCD cost itself, you should also consider the cost of related hardware, software development, RTOS, and mechanical parts. Using a low-cost microcontroller with a built-in LCD controller to drive the LCD is a clean approach, especially as more of these CPUs become available. EDN

AUTHOR'S BIOGRAPHY

Calvin Du is a senior design engineer with MedX Health Corp, where he has worked for five years. In his current position, he designs and develops phototherapy medical devices with a focus on firmware and system integration. He has a bachelor's degree from Peking University (Beijing).

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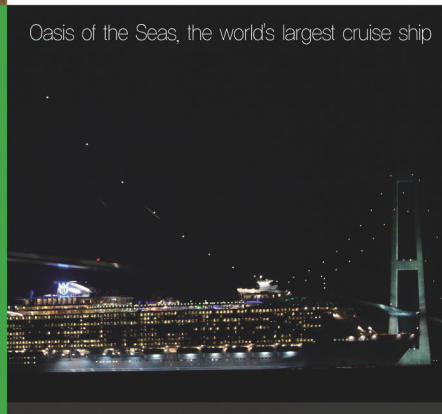

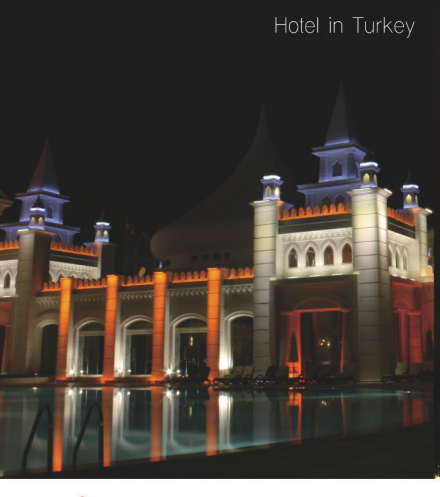

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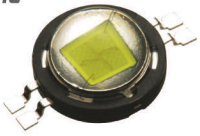

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SCRUTINIZING LED LIGHTING

A SPECIAL *EDN* SECTION

BY MARGERY CONNER, TECHNICAL EDITOR

Editor's welcome

THE LED-TECHNOLOGY SECTOR CONTINUES TO BE A GROWING INDUSTRY. BUT ITS COMPLEX DESIGN REQUIRES INTEGRATION OF SEVERAL POTENTIALLY PROBLEMATIC COMPONENTS.

Last year, while much of the world economy imploded, the LED niche held its own and even grew. For the next year, industry analysts see the market as growing at a robust 30% annual growth rate. These numbers attract new companies in search of new products for a growing market. Our goal at *EDN* is to help our design audience stay on top of trends in the market and especially the technology of HB LEDs (high-brightness light-emitting diodes).

Traditional incandescent lighting relies on relatively simply robust components that can withstand the current surges and even lightning strikes that plague ac-mains lighting. Solid-state lighting is subject to the same slings and arrows of electricity variations that any semiconductor-based part is, and designers must provide circuit protection. Faraz Hasan, global marketing and business-development manager—appliance/industrial/lighting for Tyco Electronics' Circuit Protection Business Unit, explains several circuit-protection strategies for LED-based lighting in "Circuit-protection strategies for improving LED reliability and lifetime," pg 55.

Much of the value of LED lighting comes from networking the lights into an intelligent network that can optimize a building's lighting for both efficiency and productivity. In "RF control for LED-lighting systems requires a variety of network types," pg 63, Mike Claassen, worldwide end-equipment-applications manager at Texas Instruments, looks closely at the wireless control of lighting networks and an attractive option that doesn't require rewiring a building.

Finally, in "Tear-down: inside a 7W LED light bulb," pg 69, we take a look at a straightforward 7W LED light that can serve as a replacement for a 40W incandescent and explore what components these LED lights use. It's impressive to see the complexity in what is, after all, a simple light that we're used to buying for about 50 cents at Walmart. Now, it relies on a complex design and sophisticated parts that would a decade ago have cost several orders of magnitude more.

To broaden your understanding of the interconnection of power management, sensors, and network management in LED lighting, you can watch *EDN*'s recent Webcast, "You asked for it: answers to your questions on LED lighting and network-design issues," at http://bit.ly/4JSxDj.

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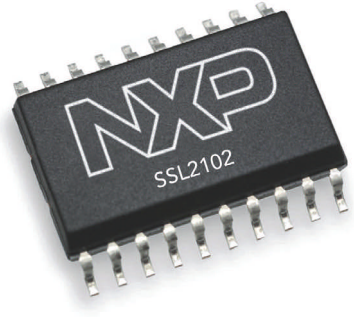

The next step in mains LED lighting

For AC mains powered LED lamps, NXP's driver and controller ICs are the next step in performance and reliability. Offering the only LED drivers available that match LED lifetimes, dimming to below 1%, support for both flyback and buck configuration, they are the solution of choice for this fast emerging market.

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BY FARAZ HASAN • TYCO ELECTRONICS' CIRCUIT PROTECTION BUSINESS UNIT

Circuit-protection strategies for improving LED reliability and lifetime

EXCESS HEAT AND SHORT-CIRCUIT FAILURES DRIVE THE NEED FOR CIRCUIT PROTECTION IN LED-BASED LIGHTING. TO COMBAT THESE FAILURES, TEMPERATURE-SENSITIVE PROTECTION DEVICES TEAM UP WITH OVERVOLTAGE PROTECTION TO HELP ENSURE LED PERFORMANCE AND RELIABILITY.

LED luminaires require precise power and heat management because LEDs convert most of the electrical energy they receive into heat rather than light. Without adequate thermal management, this heat can degrade the LED's life span and affect color output. Also, LEDs can fail short because they are silicon devices, so they may require fail-safe backup in the form of overcurrent protection.

Resettable PPTC (polymeric-positive-temperature-coefficient) circuit-protection devices have demonstrated their effectiveness in a variety of LED-lighting applications. Like traditional fuses, they limit current after they exceed specified limits. However, unlike fuses, PPTC devices can reset after the fault clears and the power cycles.

You can use a variety of overvoltage-protection devices, including MOVs (metal-oxide varistors), ESD (electrostatic-discharge) surge-protection devices, and integrated overcurrent/overvoltage devices, in a coordinated scheme with PPTC devices to help improve LED performance and reliability.

HEAT CONDUCTION

A lighting fixture using a 60W incandescent light bulb produces approximately 900 lumens of light and must dissipate 3W of heat through conduction. In comparison, using typical dc LEDs as the light source to achieve the same 900 lumens would require about 12 LEDs.

Assuming a forward voltage of 3.2V and current of 350 mA, you can calculate the input power to the LED fixture as 12×3.2V×350 mA=13.4W. In this scenario, approximately 20% of the input power converts into light, and approximately 80% converts into heat, depending on various heat-generation and other factors that relate to substrate irregularities, phonon emissions, binding, and materials.

Of the total heat an LED generates, 90% transfers through conduction. To dissipate heat from the junction of an LED, conduction is the principal channel of transfer because convection and radiation account for only about 10% of overall heat transfer. For example, an LED may convert almost 10.72W—13.40W×0.80—of heat. Of that amount, conduction transfers or removes 9.648W, or 10.72W×0.90, of heat from the junction. **Table 1** compares the efficiency, efficacy, and heat loss of various lighting methods.

TEMPERATURE EFFECT

The optical behavior of an LED varies significantly with temperature. The amount of light an LED emits decreases as the junction temperature rises, and, for some technologies, the emitted wavelength changes with temperature. If you do not properly manage drive current and junction temperature, the LED's efficiency can quickly decrease, resulting in reduced brightness and shortened life.

Another LED characteristic, relating to junction temperature, is the forward voltage of the LED (**Figure 1**). If you use only a simple bias resistor to control the drive current, forward voltage drops, and the drive current increases as temperature rises. This situation can lead to thermal runaway, especially for high-power LEDs, and cause the component to fail. It is common practice to control junction temperature by mounting the LEDs on metal-core PCBs (printed-circuit boards) to provide rapid heat transfer.

TABLE 1 LIGHTING COMPARISON

Source	Efficiency (%)	Efficacy (lumens/W)	Heat loss (%)		
			Radiation	Convection	Conduction
Incandescent	2	15	90	5	5
Fluorescent	15	90	40	40	20
High-intensity discharge	20	100	90	5	5
LED	20	75	5	5	90

PPTC devices respond quickly, limiting current to a safe level to help prevent collateral damage to downstream components.

Power-line coupled transients and surges can also reduce LED lifetimes, and many LED drivers are susceptible to damage resulting from improper dc voltage levels and polarity. Short circuits can also damage or destroy LED-driver outputs. Most LED drivers have built-in safety features, including thermal shutdown and open- and short-LED detection. However, additional overcurrent-protection devices may be necessary to help protect ICs and other sensitive electronic components.

I/O PROTECTION

A constant current drives LEDs, and their forward voltage varies from less than 2V to 4.5V, depending on the color and current. Older designs rely on simple resistors to limit LED-drive current, but designing an LED circuit using the typical forward-voltage drop that the manufacturer specifies can cause the LED driver to overheat. Overheating may occur when the forward-voltage drop across the LED decreases to a value that is significantly less than the typical stated value. During such an event, the increased voltage across the LED driver can result in higher total power dissipation from the driver package.

Today, most LED applications use power-conversion and -control devices to interface with various power sources, such as the ac line, a solar panel, or battery power, to control power dissipation from the LED driver. Designers frequently protect these interfaces from overcurrent and overtemperature damage by using resettable PPTC devices. These devices have low-resistance values under normal operating currents. In the event of an overcurrent condition, the device "trips" into a high-resistance state. This increased resistance helps protect the equipment in the circuit by reducing the amount of current that can flow under the fault condition to a low, steady-state level. The device remains in its latched position until the fault clears. Once power to the circuit cycles, the PPTC device resets and allows current flow to resume, restoring the circuit to normal operation.

Although PPTC devices cannot prevent a fault from occurring, they respond quickly, limiting current to a safe level to help prevent collateral damage to downstream components. Additionally, the small form factor of PPTC devices makes them easy to use in applica-

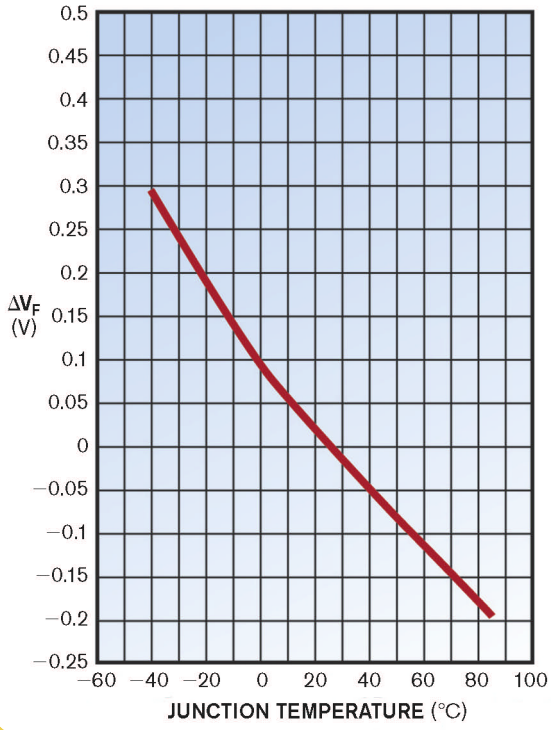

Figure 1 Forward voltage drops as junction temperature rises.

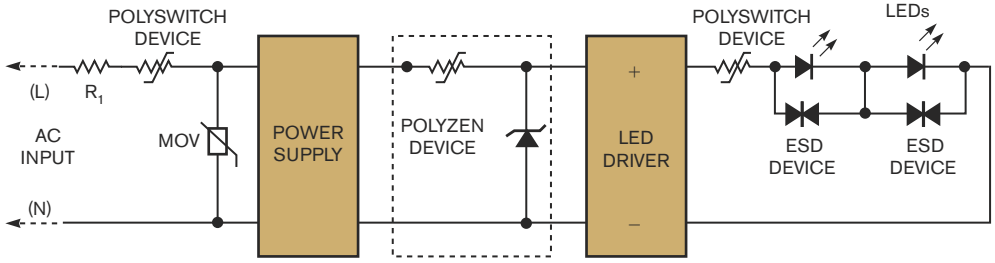

Figure 2 This coordinated protection scheme uses PolySwitch PPTC devices and MOV devices for SMPS (left), and PolyZen, PolySwitch, and ESD-protection devices for LED-driver inputs and outputs (right).

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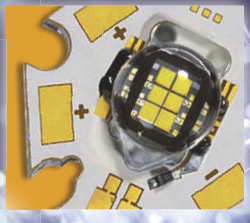

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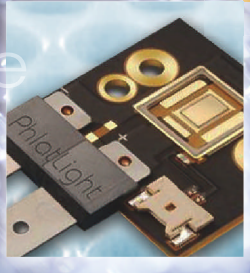

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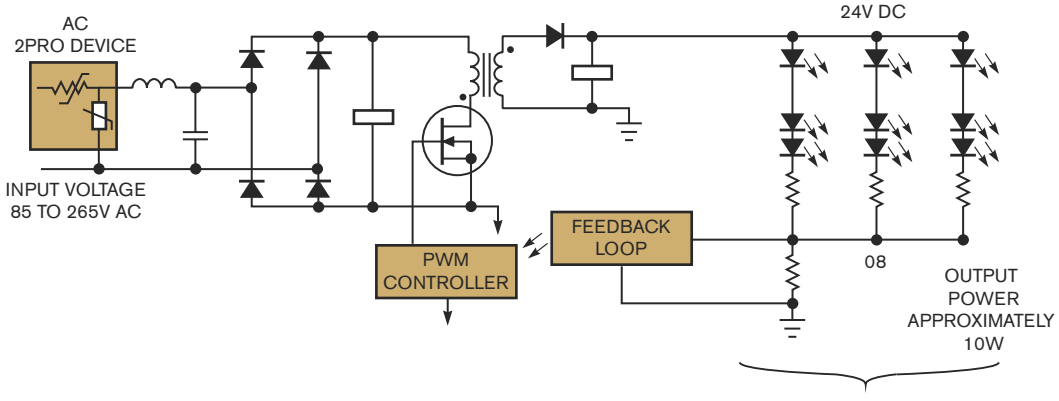
Figure 3 A typical lighting application uses an ac 2Pro device for low-power ac/dc flyback-converter protection for ac-mains LED-lighting systems. The 2Pro device combines PPTC technology with an MOV component into one thermally protected device to help provide resettability in the case of overcurrent or overvoltage events.

tions that have space constraints.

Figure 2 illustrates a coordinated protection scheme for an SMPS (switch-mode power supply) and LED-driver inputs and outputs. You can install a PPTC device in series with the power input to help protect against damage resulting from electrical shorts, overloaded circuits, or customer misuse. Additionally, you can place an MOV across the input to help provide overvoltage protection in the LED module. You can also place the PPTC device after the MOV. Many equipment manufacturers prefer protection circuits combining resettable PPTC devices with upstream fail-safe protection. In this example, R_1 is a ballast resistor



LED Lighting

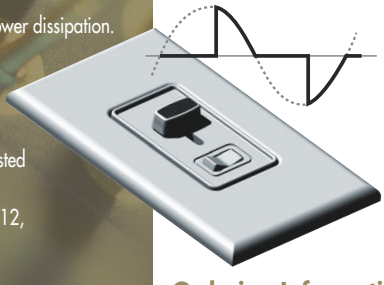
AAL404 TRIAC Dimmer Interface Controller

Features

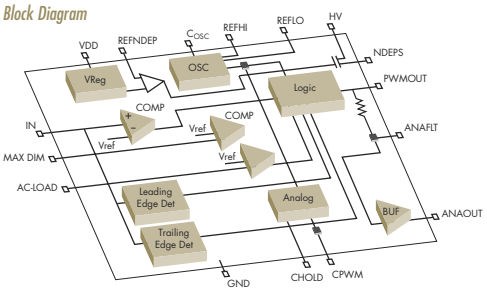
- High Voltage Linear Regulator for Digital PWM and Analog Outputs
- External control of edge-detection function
- High impedance sensing of AC input for minimum power dissipation.
- Only a single resistor needed for sensing input
- Maintains proper operation, with no dimmer input
- Upconversion frequency set by external R/C
- Input/Output PWM conversion transfer function adjusted logarithmic by external R/C
- Compatible with the IPS401, IPS402, AAL403, AAL412, and competitors LED controllers
- Adjustable Min and Max input thresholds
- High voltage depletion FET for fast start-up
- Adjustable depletion FET control for preloading and triac hold current

Application Examples

- AC/DC LED Driver Applications
- RGB backlighting
- Backlighting of LCD and PDP panels
- LED signs
- LED decoration
- Replacements for incandescent and fluorescent bulbs and fixtures
- Road signs, traffic lights



AAL1404 Block Diagram



Ordering Information

Ordering PN	Subgroup	Description	Temp. Range	Package	Packing Type	Packing Qty
AAL404 I-V28A-G-LF	Monitoring and Interface	Phase-Cut Dimming IC	Industrial	Voltage Enhanced 28-Pin QFN	Waffle Pack	28
AAL404 I-V28A-G-LF-TR	Monitoring and Interface	Phase-Cut Dimming IC	Industrial	Voltage Enhanced 28-Pin QFN	13" T&R	TBD

ASIC advantage

For samples and additional information, go to http://loci.asiacadv.com/AAL404EDN

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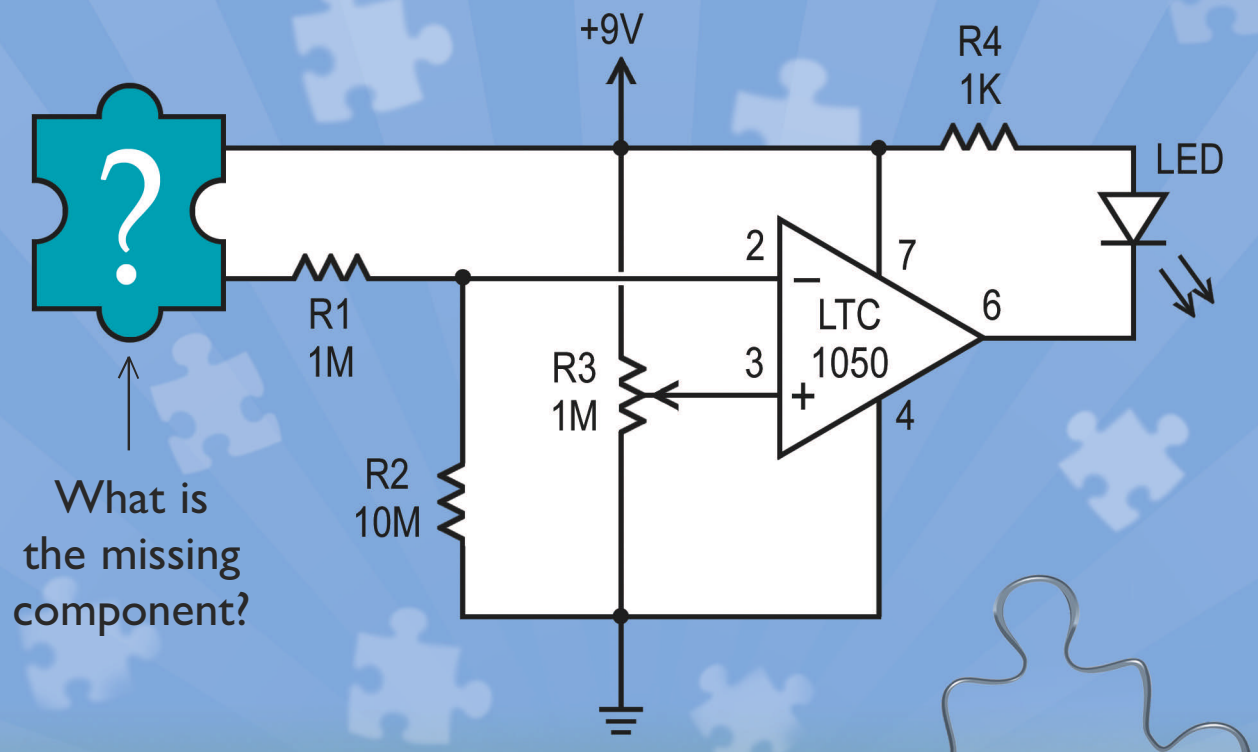
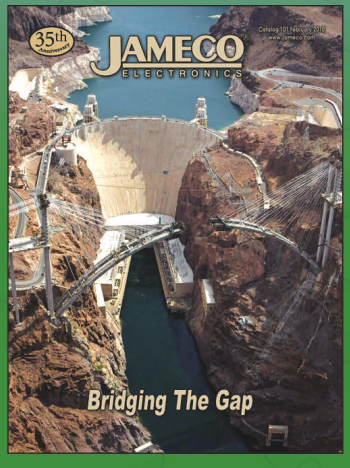


What is the missing component?



Electronics Industry guru Forrest M. Mims III has created yet another stumper. The Ultra Simple Sensors Company assigned its engineering staff to design a circuit that will trigger an LED when a few millimeters of water is present in a basement or boat. What is the water sensor behind the puzzle piece? Go to www.Jameco.com/brain5 to see if you are correct and while you are there, sign-up for our free full color catalog.

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that works with the protection circuit.

Figure 2 shows a coordinated circuit-protection design for an LED driver and an LED array. A thermally protected precision zener diode can help protect circuits from damage from overvoltage and overcurrent fault conditions. Placing such a device on the driver input offers designers the simplicity of a traditional clamping diode and obviates the need for using a significant amount of heat sinking. To fully leverage the PPTC device, you can thermally bond it to a metal-core PCB or LED heat sink. To help prevent damage from an ESD event, you can place small-form-factor, low-capacitance—typically, 0.25-pF—ESD-protection devices in parallel with the LEDs.

Designers typically use MOVs for transient-overvoltage suppression in ac line-voltage applications. New thermally enhanced MOVs help protect a variety of low-power systems against damage from overcurrent, overtemperature, and overvoltage faults, including lightning strikes, ESD surges, loss of neutral, incorrect input voltage, and power induction (**Figure 3**).

Under normal operating conditions the ac line voltage you apply to an MOV should not exceed the device's maximum ac root-mean-square voltage rating, and, if the transient energy does not exceed the MOV's maximum rating, short events clamp to a suitable voltage level. However, a sustained abnormal overvoltage or limited-current condition, such as a loss of neutral, may cause the MOV to go into thermal runaway. Designers frequently protect the MOV from thermal overheating by placing a thermal-cutoff device in series with the MOV. A typical line-voltage transient-protection scheme may also incorporate an overcurrent-protection element, such as a fuse, to protect the system from damage from an overcurrent overload that exceeds a predetermined level.

Standard unprotected MOVs are typically 275V-ac rms for a universal input-voltage range. In a loss-of-neutral condition, they can overheat—with negative consequences—even if you use a fuse or power resistor upstream. The MOV in **Figure 3**, an ac 2Pro, includes a PPTC element to help prevent thermal runaway, maintaining varistor surface temperature at less than 150°C. In the event of an overvoltage transient, such as a loss-of-neutral event, the PPTC element heats up, trips, and goes into a high-resistance state, helping to reduce the risk of MOV-device failure. EDN

AUTHOR'S BIOGRAPHY

Faraz Hasan is global marketing and business-development manager—appliance/industrial/lighting for Tyco Electronics' Circuit Protection Business Unit. He earned a bachelor's degree in mechanical engineering with honors from Aligarh Muslim University (Aligarh, India) and holds a postgraduate diploma in marketing and sales management from Bharatiya Vidya Bhavan (New Delhi, India).

LED Lighting

AAL4010 Universal Input High Brightness LED Driver

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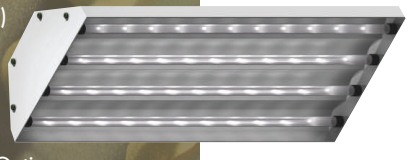
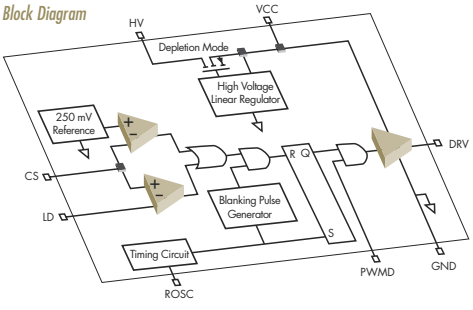


AAL1040 Block Diagram



Ordering Information

Ordering PN	Subgroup	Description	Temp. Range	Package	Packing Type	Packing Qty
AAL4010 A-V28A-G-LF	Controller	High Voltage Current Mode LED Controller	Automotive	Voltage Enhanced 28-Pin QFN	Waffle Pack	28
AAL4010 A-V28A-G-LF-TR	Controller	High Voltage Current Mode LED Controller	Automotive	Voltage Enhanced 28-Pin QFN	13" T&R	TBD

Application Examples

- Buck LED Drivers
- Backlighting (LED Flat Panels)
- Indoor/Outdoor LED Lighting
- Dimmable Display Lighting
- Constant Current Regulators

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BY MIKE CLAASSEN • TEXAS INSTRUMENTS

RF control for LED-lighting systems requires a variety of network types

THE MARRIAGE OF RF CONTROL AND LIGHTING MAKES PERFECT SENSE. WHAT'S THE BEST WAY TO MAKE THAT HAPPEN?

It's an attractive idea to be able to control a relatively remote device, such as a light, using a small, portable controller, such as a light switch, without running a network of wiring. A cursory investigation into the requirements of the lighting industry points to ZigBee's mesh-networking capability as a leading candidate for this role because it addresses most of the requirements of today's lighting systems and provides a set of capabilities for the future. For other styles of lighting systems, however, ZigBee is not necessarily ideal (see **sidebar** "Network applications").

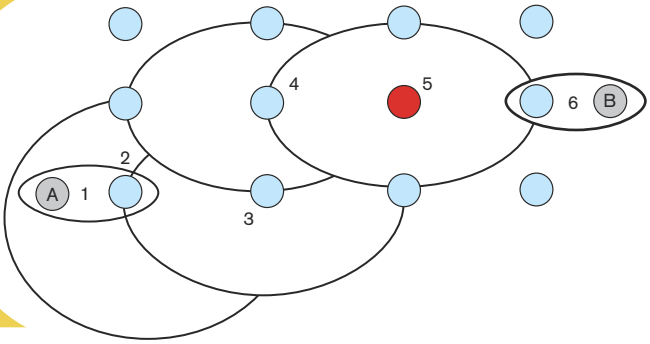
BUSINESS LIGHTING

Most people work or have spent time in large buildings with few walls and many rows of lighting that, for the most part, are indistinguishable from each other. When you combine these rows, they can light a large open space. During such a lighting system's lifetime, it is active 10 to 12 hours a day to keep light on for the building's occupants as they go through their workday. At night, a subset of these lights remains active, providing a level of security for the building and its contents. A typical ZigBee network can control a large, uniform area of lights (**Figure 1** and **Reference 1**).

The network has a coordinating device, a router, and an endpoint. The coordinating device establishes the network and controls how the devices in the network interact with each other. After establishing the network, the coordinator's work is done, and it can disappear from the system, although it usually reverts back to the function of a router.

A router simply routes messages across the network. The router is responsible for delivering messages that come from or are going to the router's child devices—other routing or end devices that the router has joined to the network. Messages that are not going to the router's child devices propagate the message through the network to its intended recipient. For the network to function properly, the routing devices must be in RF range of another routing device and continuously listening for new messages coming through the network.

End devices are typically long-life-battery-powered ZigBee nodes that users can power



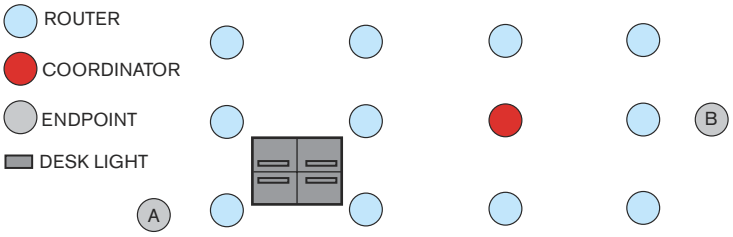


Figure 2 The network message propagates through the network for reception by End Device B on the sixth transmission, or hop. The main purpose of the command is to activate the lights on each of the routers, which this message also accomplishes.

Figure 1 A typical ZigBee network can control a large, uniform area of lights. For the network to function properly, the routing devices must be in RF range of another routing device and continuously listening for new messages coming through the network.

down; therefore, they require less power than do coordinators and routers. Because these devices are not always in receive mode to listen for messages, they cannot serve as routers in the ZigBee network. Instead, they act as child devices to a router and depend on the router to deliver and receive any messages. In a lighting system, typical end devices can be light-level or presence-detection sensors or, more traditionally, light switches. The desk lights in **Figure 1** are light controllers, but they can also be end devices. They can become child devices of the routers and still be able to receive the light commands from the parent device.

End Device A is a light switch. Upon its activation, it sends a message to End Device B, a presence-detector sensor, which acknowledges the issuance of a light-on command. The command message repeats throughout the network to all of the nodes to End Device B on the sixth transmission, or hop (**Figure 2**). The main purpose of the command is to activate the lights on each of the routers, which this message accomplishes.

Message propagation isn't the only feature of a mesh network. Consider adding or modifying a room using its lighting network, which can possibly block the connection between nodes. **Figure 3** shows the lighting system with the addition of a large HVAC (heating/ventilation/air-conditioning) duct that blocks

NETWORK APPLICATIONS

Even though the coordinating and routing functions of a ZigBee stack use many instruction cycles for the host processor, this processor should have enough leftover instructions to perform other functions, such as controlling a light. Therefore, a single lighting-control processor can serve two purposes: controlling the light and routing the ZigBee messages.

In a typical wireless system, the function requiring the most power comes from the RF operation, with the transmitting and the receiving stages typically requiring the highest power and the second-highest power, respectively.

The activated microprocessor follows the RF stage as the next-highest power-demand stage. ZigBee routing devices typically pull an average of approximately 25 mA, or 75 mW, which is low for a node controlling a 100W light bulb.

The requirement for 75 mW of power for a routing node prevents ZigBee from use in applications with small power sources. In comparison, devices in sleep mode, depending on their usage, can pull less than 1 mW of power.

Shorter wavelengths associated with higher carrier frequencies are more reflective than longer wavelengths. For that reason, 2.4 GHz is a more desirable carrier frequency for a single-room system because the walls in the room greatly attenuate the signal outside the room.

The reflectivity of the signal also helps to propagate the carrier around RF sink, such as the human body, to help compensate for possible nulls in the room.

Learn more about ZigBee at www.ti.com/zigbee-ca. For TI's complete portfolio of lighting products, visit www.ti.com/led-ca.

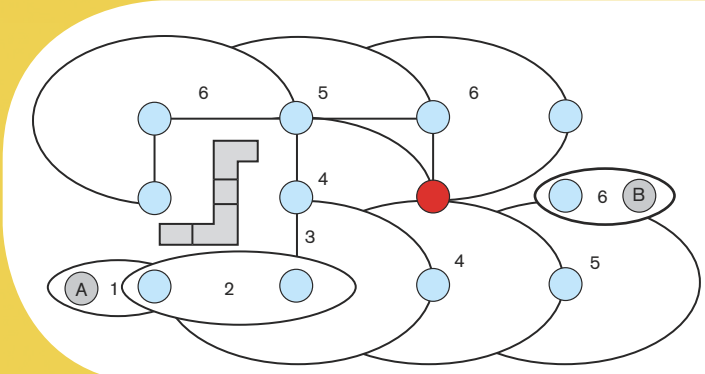


Figure 3 This version of the lighting system adds a large HVAC duct that blocks RF communications between the nodes it intersects. Even though the duct cuts the path in half, both sides can route the messages through the entire network.

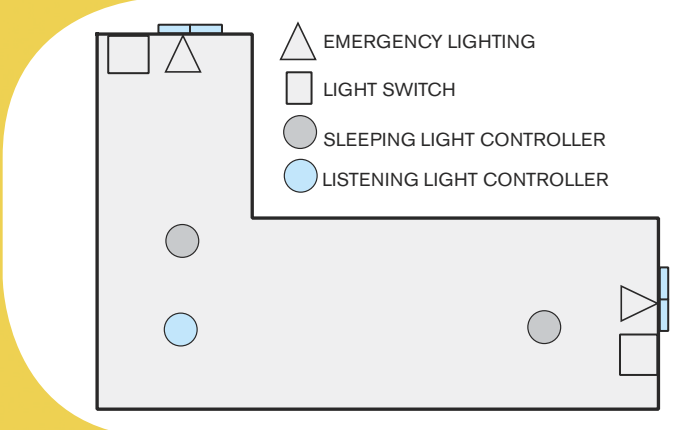


Figure 4 This conference-room lighting system has multiple constantly powered ceiling lights as well as an emergency-lighting system over the exits. ZigBee can work in this system, in which a cluster tree beacons the network, allowing the sleeping nodes a defined time to accommodate priority messages.

RF communications between the nodes it intersects. Even though the duct cuts the path in half, both sides can still route the messages through the entire network. The ability to work around either permanent or intermittent changes in the network's RF path highlights the healing capability of a ZigBee network.

ROOM LIGHTING

Conference or training rooms present a different set of lighting considerations. These lighting systems don't require a message to propagate across a large span of lights. They instead have the opposite requirement: the control of only the lights in the room. Controlling lighting outside the room is an undesirable effect and serves as an RF-jamming source for the external controllers.

Figure 4 shows a lighting system in a conference room with multiple constantly on ceiling lights and emergency lighting over the exits. Whatever causes an emergency, however, may disrupt the power, and the system will remain as low power as possible to keep the emergency lights active for as long as possible. The portable and low-power light switches typically interact with the system once or twice an hour.

In this instance, all the devices are within range of each other and, therefore, require only one device to receive while other devices can poll or go into sleep mode. A star-network topology would allow all devices to communicate through the active node. This configuration yields significant power savings for the light switches and the emergency lights, but the polling cycles increase the response time of the sleeping nodes.

A ZigBee network could work in this system, too. In that scenario, a cluster tree would beacon the network, allowing the sleeping nodes a defined time to accommodate priority messages. This approach enables the network to reduce power on the child devices and still allow a periodic check for alarm or lighting-level-change requests.

LINEAR LIGHTING

Neither a star nor a traditional mesh network can address the lighting system in **Figure 5**. In this instance, a message—typically, "light not functional"—must transmit linearly and in the appropriate direction over a large distance to a node that can report the outage. When a light stops functioning, the municipality must receive a message to send a technician from the address of the inoperable light to the address of the municipality through a series of point-to-point messaging from the other lights.

If the lights are line-powered, the radio can be consistently in receiving mode, waiting for a message to relay. In this mode, the latency of the message is only hundreds of milliseconds per hop. If the lights are solar-powered, power becomes more important, and the devices can enter a periodic-receive mode. You must synchronize this mode with the transmission of the other node, which is more complicated, however. Also, you must take the polling period into consideration when calculating the time between message hops.

Figure 6 shows how the message arrives at its destination. Node B reports the light-out message to Node F by sending a point-to-point message to Node C. When Node C gets the message, it knows that the message originated at Node B because there is no history, and the message is intended for Node F. At that point, Node C also knows the direction the message must transmit, which is away from Node B, or toward Node D. In the second hop, Node C sends the message to Node D and places Node B in the history of the packet to tell Node D which direction it should transmit.

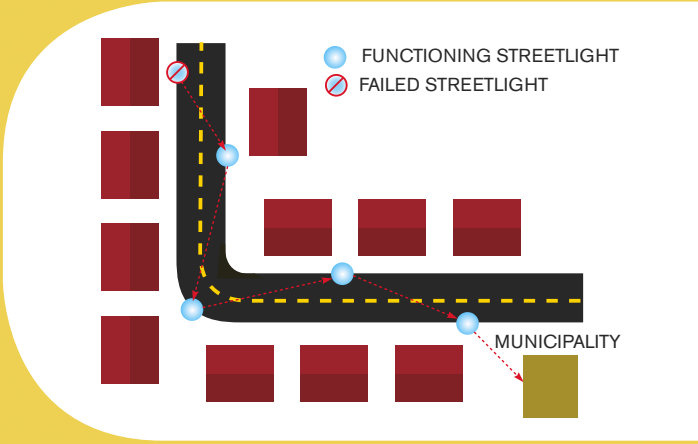
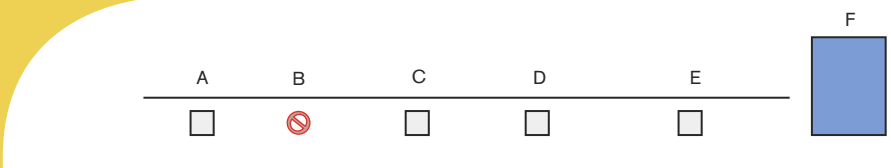


Figure 5 Neither a star network nor a traditional network can address a message-relay lighting network. A message such as "light not functional" must transmit linearly and in the appropriate direction to a node that can report the outage.



	DESTINATION	SOURCE	FINAL	HISTORY	MESSAGE
HOP 1:	C	B	F	NULL	LIGHT B OUT
HOP 2:	D	C	F	B	LIGHT B OUT
HOP 3:	E	D	F	C	LIGHT B OUT
HOP 4:	F	E	F	D	LIGHT B OUT

Figure 6 In this instance of a message-relay network, each node must learn its neighbor's address in the network's discovery phase. If a node goes down, the chain cannot be broken; otherwise, the message cannot be relayed.

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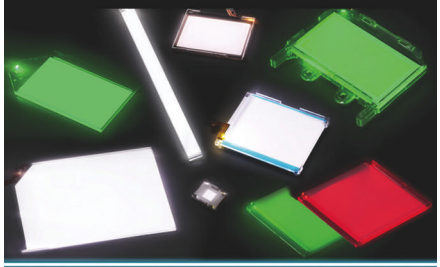

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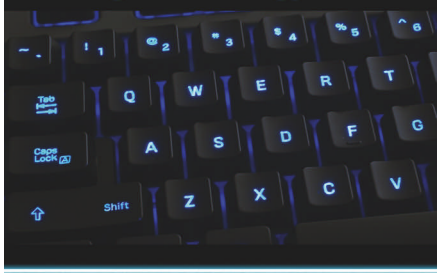

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Two hops later, the message arrives at Node F.

Two things quickly become apparent in this network. First, each node must automatically learn its neighbor's address in a discovery phase in the network. The process must be automatic because of the number of nodes and length of time it would take to accomplish this task manually. Second, the message must reach its destination even if a node goes down, so there can be no broken links in the chain.

Figure 7 shows the discovery phase of Node C. Node C sends a broadcast message at a low-power transmission, soliciting a response from the other nodes. Nodes B and D should respond. Node C now knows that its nearest neighbors are nodes B and D, so it should expect to see messages from those two nodes in its routing tables. Node C then increases its transmitting power and sends another broadcast. Nodes B and D respond again, as do nodes A and E. Node C is now aware of nodes A and E as its second-closest neighbors. Finally, Node C ups its transmitting power to its maximum and does a final broadcast. As you would expect, nodes A, B, D, and E respond, as does Node F. There is no other node past Node A, so no other node should respond.

In this small-scale example, the nodes discover the entire network, showing how the device learns about its neighbors. After this process, all the devices know their neighbors but do not know their neighbors' direction. They can determine a direction by relaying a message from the head node, Node F, which is the municipality, through the network to the node at the end, which is Node A, and then back to Node F.

This approach serves two purposes. It allows the nodes in the network to discover the direction of their neighbors, and it tells Node F where the network ends—Node A. In the example, Node C now knows that, to communicate with Node F, it must send a message to Node D. If Node D is in the history of the transmission, it should send the message to Node B.

In normal operation, the nodes communicate with their nearest neighbors at −10 dBm (decibels referenced to milliwatts). This approach saves power for the node and maintains the network's health. If Node C stops functioning, nodes B and D can communicate over it by increasing their power. Node D should report to the municipality that Node C has stopped operating. The distance between the nodes and the latency—the number of relays between the initiating node and the final-destination node—essentially limit the network's range.

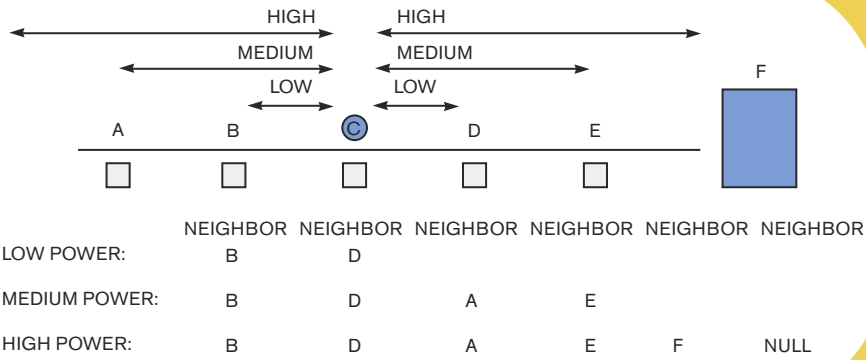


Figure 7 In its discovery phase, Node C broadcasts at increasingly higher power levels to find its neighbors.

Established protocols, such as ZigBee, take into account many of the needs of a typical lighting system.

All of these examples are real-world applications in the lighting world. Each has a set of different requirements. They all have common requirements in that RF robustness is a must for a system to function appropriately, and they will find use in environments with a lot of possible variables that will affect that robustness.

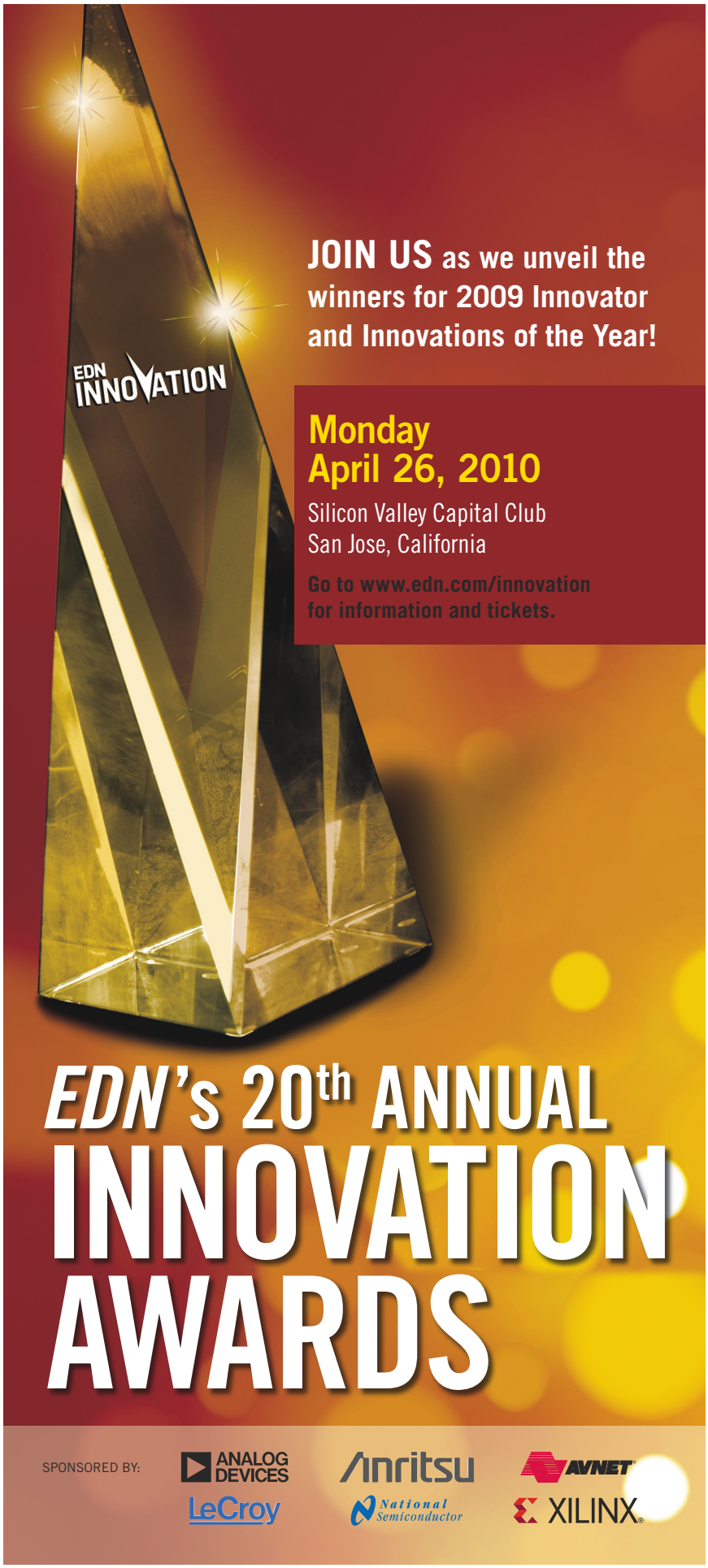
Established protocols, such as ZigBee, take into account many of the needs of a typical lighting system. The features of ZigBee make it a versatile and effective option for the industry. In some applications, however, a simpler star network allows for lower-powered nodes and a simpler implementation. In other applications, neither ZigBee nor star networks are viable alternatives due to their range or hop constraints. In these systems, a more proprietary network tailored to the needs of the system is more appropriate. EDN

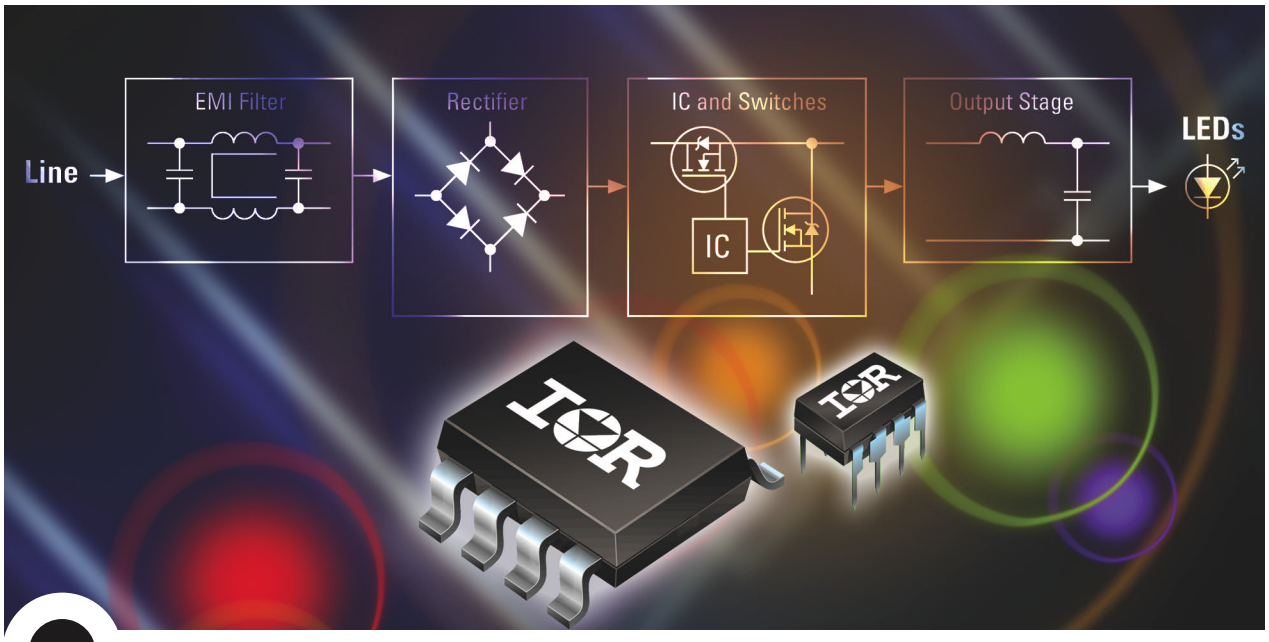
REFERENCE

1 "RF/IF and ZigBee solutions," Texas Instruments, http://focus.ti.com/analog/docs/gencontent.tsp?familyId=367&genContentId=24190&DCMP=hpa_contributed_articles&HQS=ArticleReprint+OT+zigbee-ca.

AUTHOR'S BIOGRAPHY

Mike Claassen is the worldwide end-equipment-applications manager at Texas Instruments, where he is responsible for system-level integration of TI's semiconductor portfolio. He has trained hundreds of design professionals in implementing the low-power-RF portfolio in their applications. Claassen received a bachelor's degree in electrical engineering from Kansas State University (Manhattan, KS).





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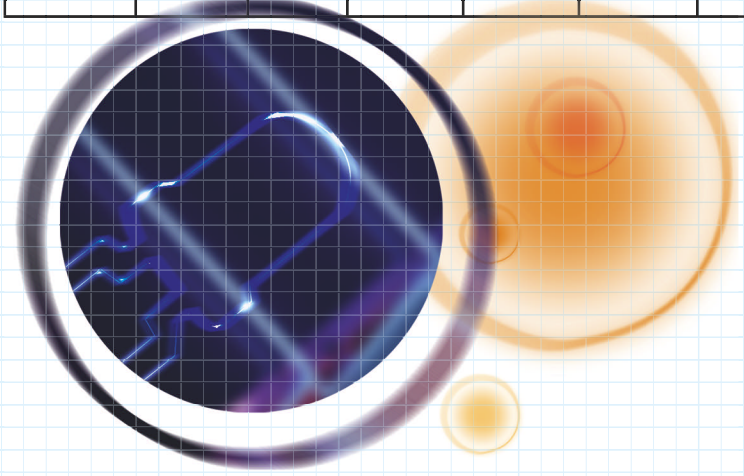

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Figure 1 Glue secures the light's plastic bulblike cover.

BY MARGERY CONNER, TECHNICAL EDITOR

TEAR-DOWN: inside a 7W LED light bulb

TESS (www.tesscop.com), a Taiwanese manufacturing company, recently introduced a 7W LED bulb that, at 560 lumens, can serve as a replacement for a typical 500-lumen, 40W incandescent bulb (**Figure 1**). TESS has received UL (Underwriters Laboratories) approval for the light and can begin selling it in the United States. It expects each light to sell for about $22.

TESS obligingly sent me two samples of the light—one 5000K version in cool white and one 2700K version in warm white. The warm-white version produces 450 lumens. These nondimmable bulbs are not direct replacements for 40W incandescent devices.

I put the warm-white bulb to a subjective test by using it in a table lamp that formerly used a 40W CFL (compact-fluorescent-light) bulb. Although the LED has a more directional light, which it casts over a 120° angle, it worked in the lamp. It has a barely noticeable hum that you can hear at 18 in. or closer. The chief charm of the light is that it's instant-on: There's no warm-up period that a CFL requires. The specified L70 lifetime of the light is 10,000 hours, whereas the specified lifetime of a CFL is 8000 hours. The CFLs in my house routinely fail after about two years of service.

I was happy with the warm-white LED's color, so I decided to use the cool-white light as the sacrificial lamb to see what's inside. The plastic dome is glued onto the finned aluminum base that acts as a heat sink for the LEDs. (The product's box says the LEDs are from Cree.)

The bulb holds seven LED packages and two empty pads (**Figure 2**). TESS has announced plans to offer a 9W bulb and will probably use the same PCB (printed-circuit board) by adding two more LEDs on the empty pads. The specks dimly visible in the yellow centers of the LEDs show that each LED is really a package of multiple LED chips (**Figure 3**). The plastic-looking gray pad around the PCB's edges in **Figure 2** is a thermal conductive pad for better thermal transfer to the aluminum heat sink.

The hollow base of the heat sink encompasses the light's power-control circuit (**Figure 4**). A silver-colored clip-on heat sink on the HB-LED-driver IC is an MIP552 that Panasonic introduced in 2007. You can see more gray thermal conductive pad, appar-

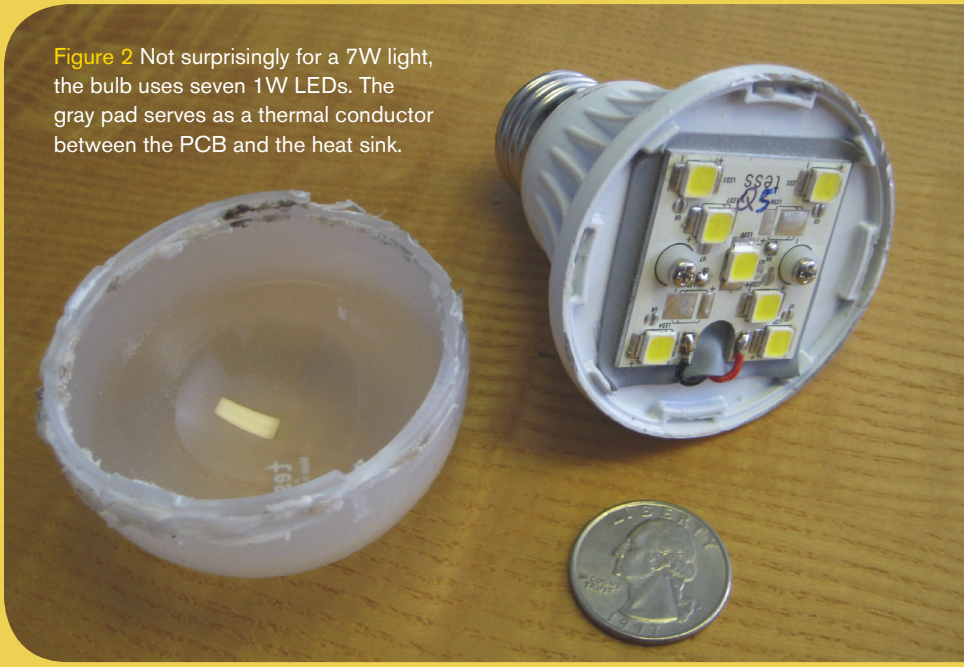

Figure 2 Not surprisingly for a 7W light, the bulb uses seven 1W LEDs. The gray pad serves as a thermal conductor between the PCB and the heat sink.

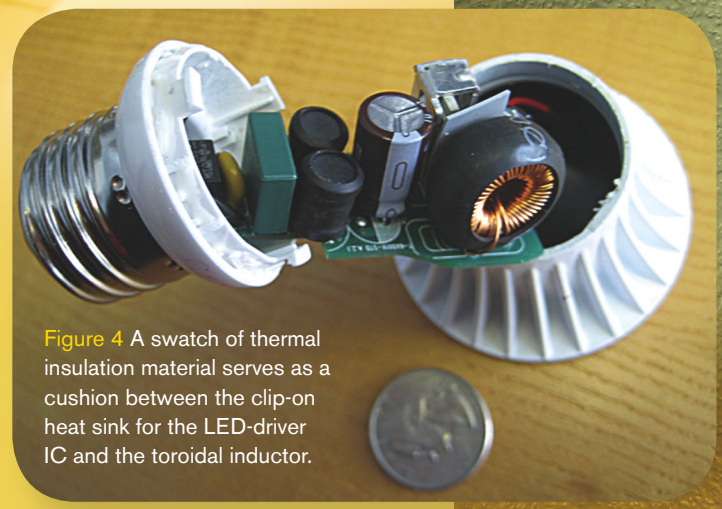

Figure 4 A swatch of thermal insulation material serves as a cushion between the clip-on heat sink for the LED-driver IC and the toroidal inductor.

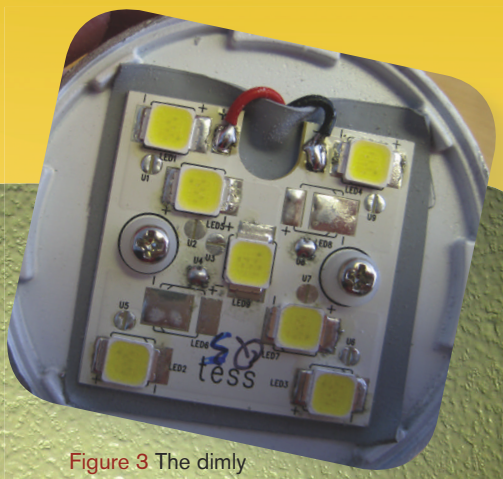

Figure 3 The dimly visible dark specks are the tiny LED chips that compose a 1W LED package.

ently to protect the two components from mechanical vibrations or shock if they rub together, between the toroidal inductor and clip-on heat sink. The MIP552 is dimmable, but the dimming feature almost doubles the number of necessary surrounding passive components and wouldn't fit inside the light's current form factor. The spec sheet lists the LED driver's switching frequency as 44 kHz.

The light still worked after I took the photos and reassembled it. However, gluing or taping the plastic dome on top didn't seem like such a good idea for use in an easily accessible table lamp. It now has a home in the laundry room, where it's one of three lights behind a light fixture and its exposed guts are less of a hazard (**Figure 5**).

Figure 6 shows the difference in color temperature between the cool-white, 5000K LED light and the warm-white, 2700K CFLs. Do I like the LED lights? You bet. If price were no object, I would replace all 40W CFLs in the house with LEDs. EDN

Figure 6 The cool-white light is evident in comparison with the warm-white CFLs. The LED light also comes in a 2700K version.

Figure 5 The exposed light finds a new home in a protected ceiling fixture.

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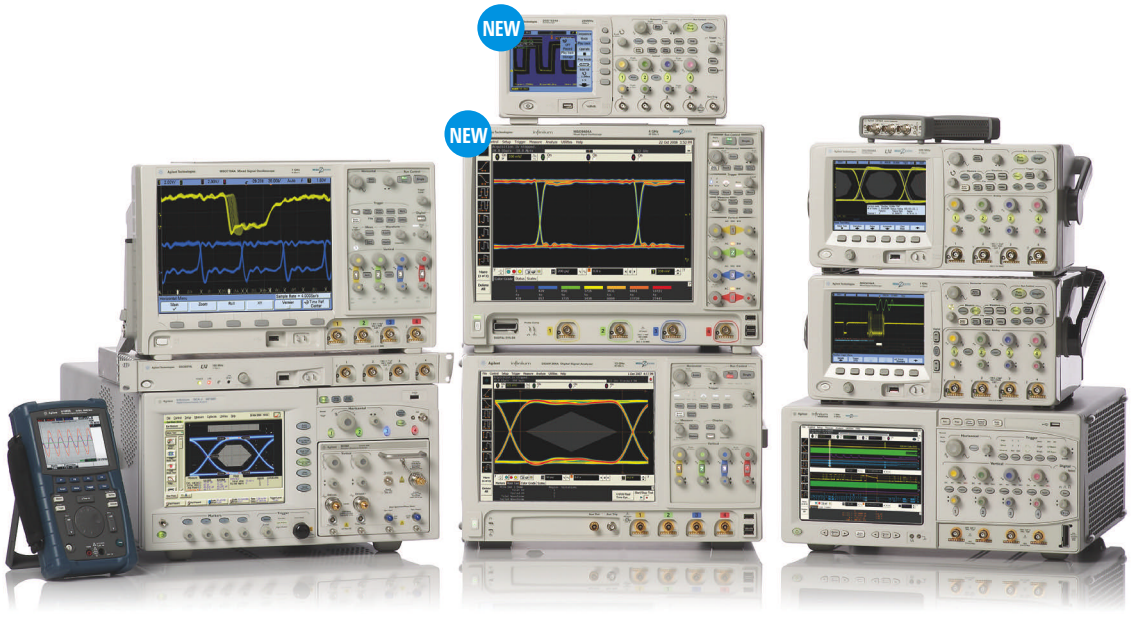

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READERS SOLVE DESIGN PROBLEMS

Strategy processes video in RAM

Yu-Chieh Chen and Tai-Shan Liao,
National Applied Research Laboratories, Hsinchu, Taiwan

Many video devices, such as the Analog Devices (www.analog.com) ADV7179 DAC, have analog-baseband-TV interfaces for PAL (phase-alternating-line) and NTSC (National Television System Committee) video signals. Unfortunately, these kinds of DACs accept video in interlaced-image format only, but you may need progressive-scan video instead. Furthermore, many of the progressive-scan images vary in size, which makes it more difficult to convert a progressive-scan image to an interlaced image. Therefore, you need a universal and efficient image buffer, such as SDRAM or DRAM, as a strategy for separating the image field.

Figure 1 shows the timing for a typical progressive-image data format. The upper four signals include the progressive-image source, including a frame-synchronization signal, a line-synchronization signal, a signal, and a pixel clock with pixel-image data. The lower two signals are the frame-synchronization signal, which contains many line-synchronization signals when the frame-synchronization signal is high, and the line-synchronization signal.

The pixel clock writes the progressive-image data into FIFO (first-in/first-out) memory. A higher-rate data clock can then write the data into RAM when each line-synchronization signal is low. This procedure ensures that the progressive-image data will correctly write into SDRAM regardless of how the pixel clock changes because of the various progressive-image data sizes. When the RAM write-enable signal or RAM read-enable signal is high, the system writes data into or reads data from SDRAM.

Figure 2 shows the frame-synchronization signal of progressive-image data and the frame-synchronization signal of interlaced-image data. The write-new-data and read-old-data enable signal executes at every line-synchronization signal of the progressive-image data when at a low level and at every frame-synchronization signal when at a high level. You can execute the read-old-data enable

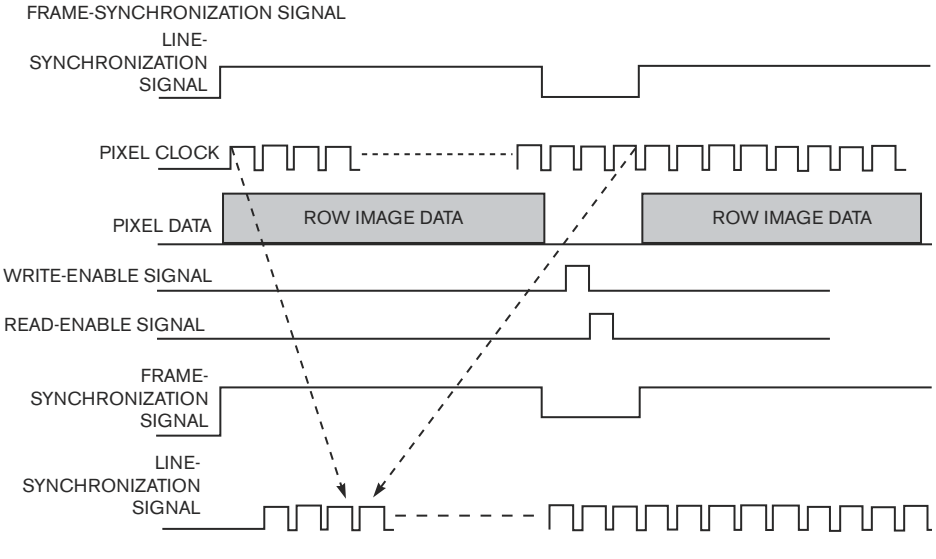

Figure 1 The pixel-clock signal puts image data into FIFO memory, which later synchronizes and goes into system RAM.

DIs Inside

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signal only when the frame-synchronization signal is low, however. This scenario occurs when there are no valid image data in this period. **Figure 3** shows the data flow of the SDRAM-accessing procedure. A frame may, for example, contain 15 rows, in which you define the row data to count from 00 to 0e. Image data for odd rows are one, three, five, seven, nine, 11, 13, and 15, and image data for even rows are two, four, six, eight, 10, 12, and 14.

By using this SDRAM-accessing strategy, you can generate the interlace data and synchronize it with the frame-synchronization signal of the original progressive data. Thus, you need not worry about image size. Moreover, it can easily tune the interlaced-image data timing, changing the number of blank rows, without changing the write-into- or read-from-SDRAM sequences. You need to decide only which line-synchronization signal in low-level periods reads the old image data from the SDRAM. EDN

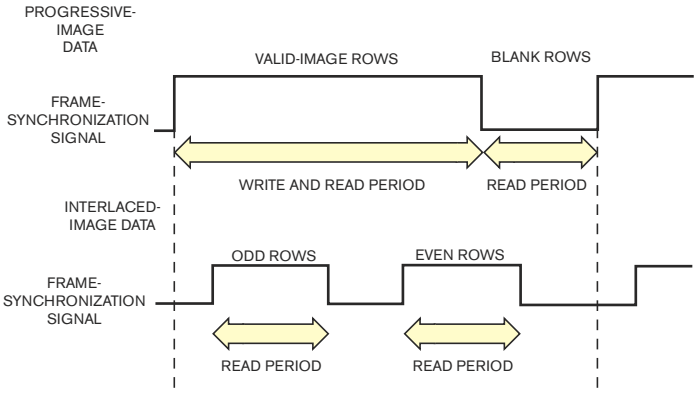

Figure 2 The frame-synchronization signal of progressive-image data alternates between reading odd and even rows of data in memory.

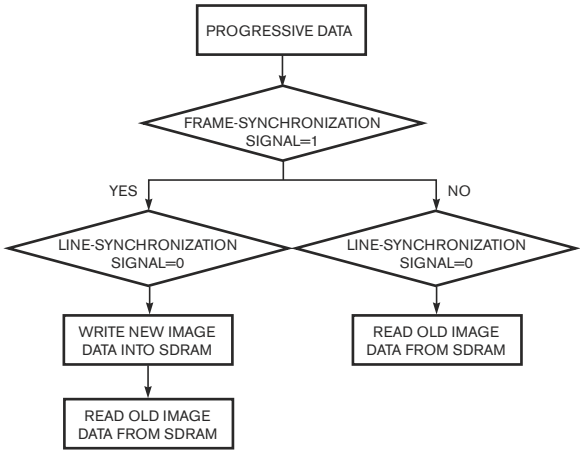

Figure 3 The state of the frame-synchronization signal determines whether the system performs a read or a write operation.

Rectangular-waveform generator produces 25 and 75% duty cycles

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

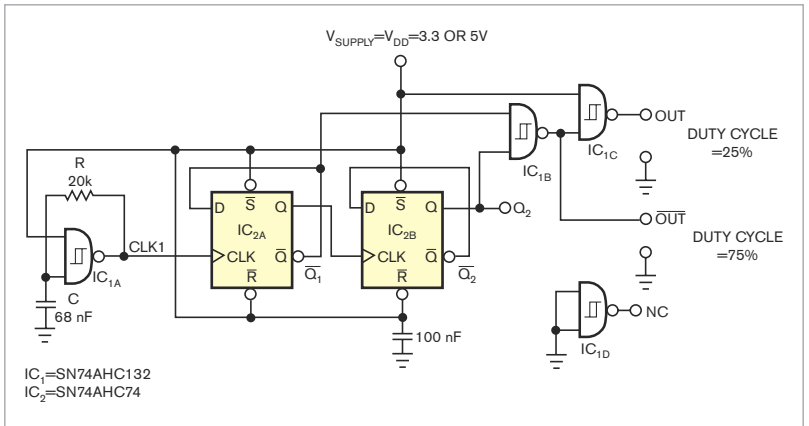

Figure 1 This circuit uses two flip-flops and three NAND gates to generate waveforms with 25 and 75% duty cycles.

Test applications may call for a rectangular waveform having a precision duty cycle higher or lower than 50%. The circuit in **Figure 1** is a free-running generator using just two ICs that produces rectangular-waveform duty cycles of both 25 and 75%. It holds the duty-cycle accuracy regardless of the duty-cycle accuracy from the signal source, an oscillator circuit comprising a Schmitt-trigger input NAND gate, IC_{1A}. Flip-flop IC_{2A} divides the oscillator's frequency by two at its $\overline{Q_1}$ and Q_1 outputs. Flip-flop IC_{2B} functions as a modulo-two divider clocked from the Q_1 output of IC_{2A}. Thus, IC_{2A} and IC_{2B} divide the oscillator's output by four.

NAND gates IC_{1B} and IC_{1C} generate the output waveform from the $\overline{Q_1}$ and Q_2 signals. **Figure 2** shows the output from NAND gate IC_{1B}. You can generate the 25% duty cycle by simply re-

High-voltage integrated pulsers and switches save space and reduce power consumption

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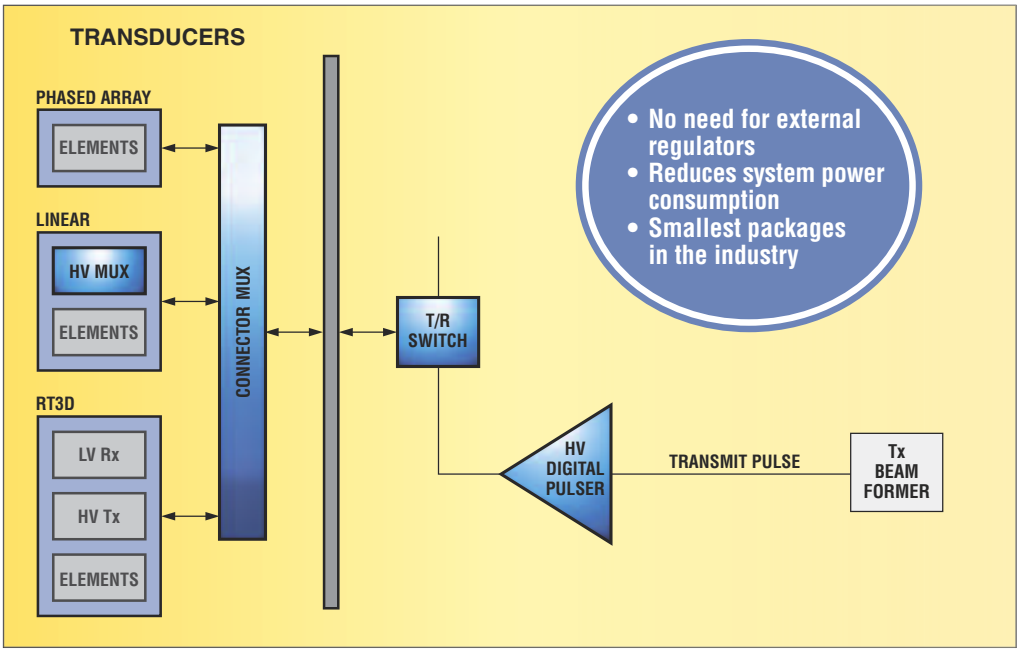

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placing the waveform that IC_{1B} outputs with the one that gate IC_{1C} outputs. If the active level is low instead of high, you can simply interchange the outputs of IC_{1B} and IC_{1C}.

The repetition frequency, $1/T_{REP}$, of the oscillator employing IC_{1A} is almost independent of the supply voltage within the range of 3 to 5V because both the positive and the negative thresholds of the input CMOS Schmitt trigger are roughly proportional to the supply voltage. Rough analysis gives a repetition frequency of approximately $2.7/\tau$, where $\tau=RC$, the time constant of the RC circuit around gate IC_{1A}. Further, the oscillator's waveform duty cycle is approximately 46.3%. EDN

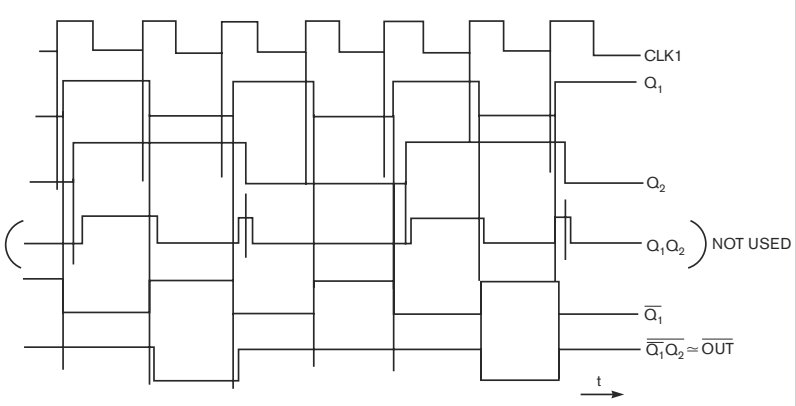


Figure 2 NANDing the $\overline{Q_1}$ and Q_2 logic signals gives a glitch-free output.

Battery simulator has variable ESR response

Barry Galvin, Grae LLC, Simi Valley, CA

You may lack experience and hardware when designing battery-operated products. The battery life of a product can depend more on the ESR (equivalent series resistance) than the terminal voltage. This situation is especially true when you use switching regulators to boost the battery voltage. The switching regulator creates a higher load as the battery voltage decreases. The ESR of a real battery is not constant. When you

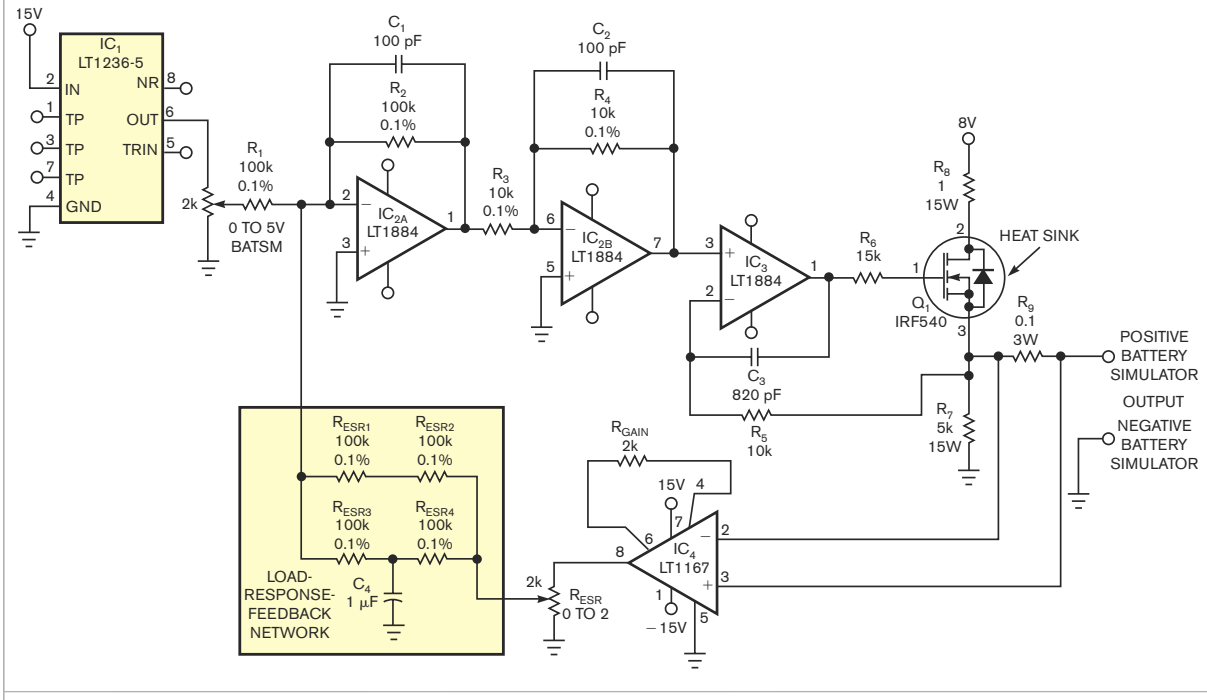


Figure 1 This simulator circuit represents the load response of many battery types.

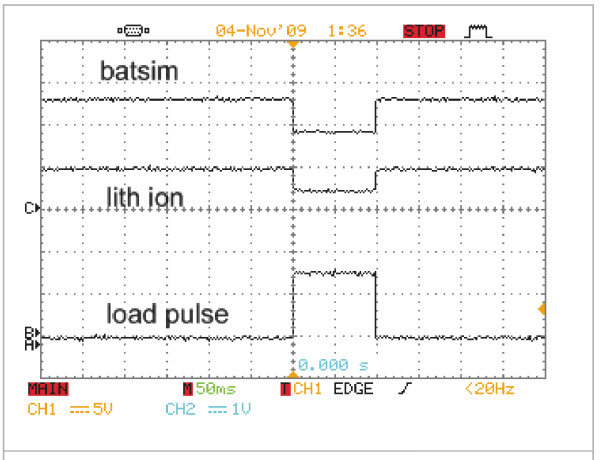


Figure 2 With no feedback capacitor, the simulator closely matches the response of a large lithium-ion battery.

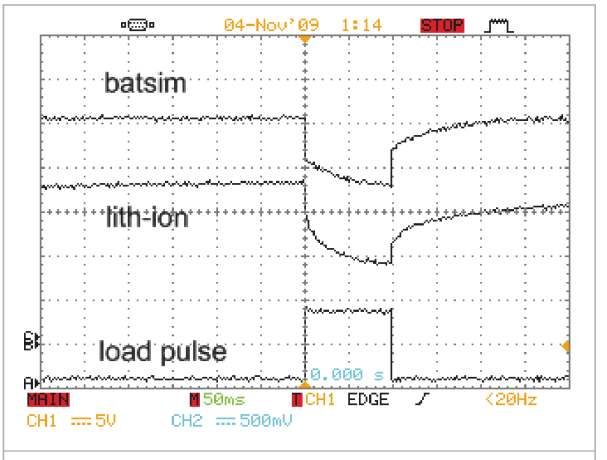


Figure 3 Adding capacitive feedback causes the simulator to act like a much smaller battery.

remove a battery load, it reacts and "heals" as its ions rediffuse. Portable electronics may include a low-power or a sleep mode. The device takes short high-power pulses from the battery.

The battery simulator in this Design Idea duplicates a battery's ESR-response curve. If you place different values in the feedback network, you can obtain various ESR curves. The circuit simulates most battery types, including lithium ion and alkaline. It supplies 0.5 to 4.2V at several amperes to the device under test, and it can simulate the ESR of a variety of battery types. You can change the delay to the final value of ESR by setting the ESR potentiometer. Some battery types exhibit this unique characteristic. It has a large influence on the delivery of pulsed current to a load.

In the circuit, IC_1 supplies a stable voltage, setting the unloaded output voltage (**Figure 1**). IC_2 provides the necessary inversions for the ESR function. IC_3 and Q_1 form a power-output stage that receives a voltage of 8V. Resistor R_8 limits the power. IC_4 senses the output current through R_9 and provides a gain of 20. This signal goes to the ESR timing circuit, providing both the ESR effect and the response timing.

You can simulate battery chemistries and sizes by varying the component values. If you omit C_4 and replace R_{ESR1} through R_{ESR4} with one 100-kΩ resistor, only the basic ESR function results. **Figure 1** omits power and bypass capacitors.

Applying a 1A load pulse without the capacitor in the feedback network causes the simulator response to closely follow the response of a 2000-mAhr lithium-ion 18650 battery (**Figure 2**). You can also add the capacitor to the feedback network to make the simulator better represent the response of a small, 200-mAhr lithium-ion battery (**Figure 3**). With proper adjustment of the circuit, you can produce many response curves. You can download National Instruments' (www.ni.com) LabView software and the voltage-ESR curves of selected battery types from Grae LLC (www.graellc.net).EDN

Create LED-lighting patterns without a controller

Jeff Tregre, www.BuildingUltimateModels.com, Dallas, TX

This Design Idea describes a simple LED-lighting-effects circuit comprising only five chips and costing only a few dollars. When you first observe the circuit in action, you will think that it uses a PIC (peripheral-interface-controller) chip requiring you to program hundreds of lines of code to generate the lighting effects. You can view the lighting effects in a video with the Web version of this Design Idea at www.edn.com/100318dia.

The circuit comprises seven functional blocks (**Figure 1**). IC_1 is an LM556, which has two 555 timers in one package. The first timer produces the main clock frequency of approximately 0.105 Hz. It toggles high to low approximately every 10 seconds. The polarity of the clock's signal changes the frequency of the VCO (voltage-controlled oscillator) that makes up the other half of IC_1 from low to high. Resistor R_2 and capacitor C_2 set the clock frequency. Changing either component changes the frequency.

The output from the first 555 timer feeds the control voltage input on the second 555 timer, letting it function as a VCO whose output frequency ranges from approximately 10 Hz when the first 555 timer output is high to approximately 33 Hz when the output is low. Components R_4 and C_3 set the VCO's frequency, and R_6 and C_4 control the smooth transi-

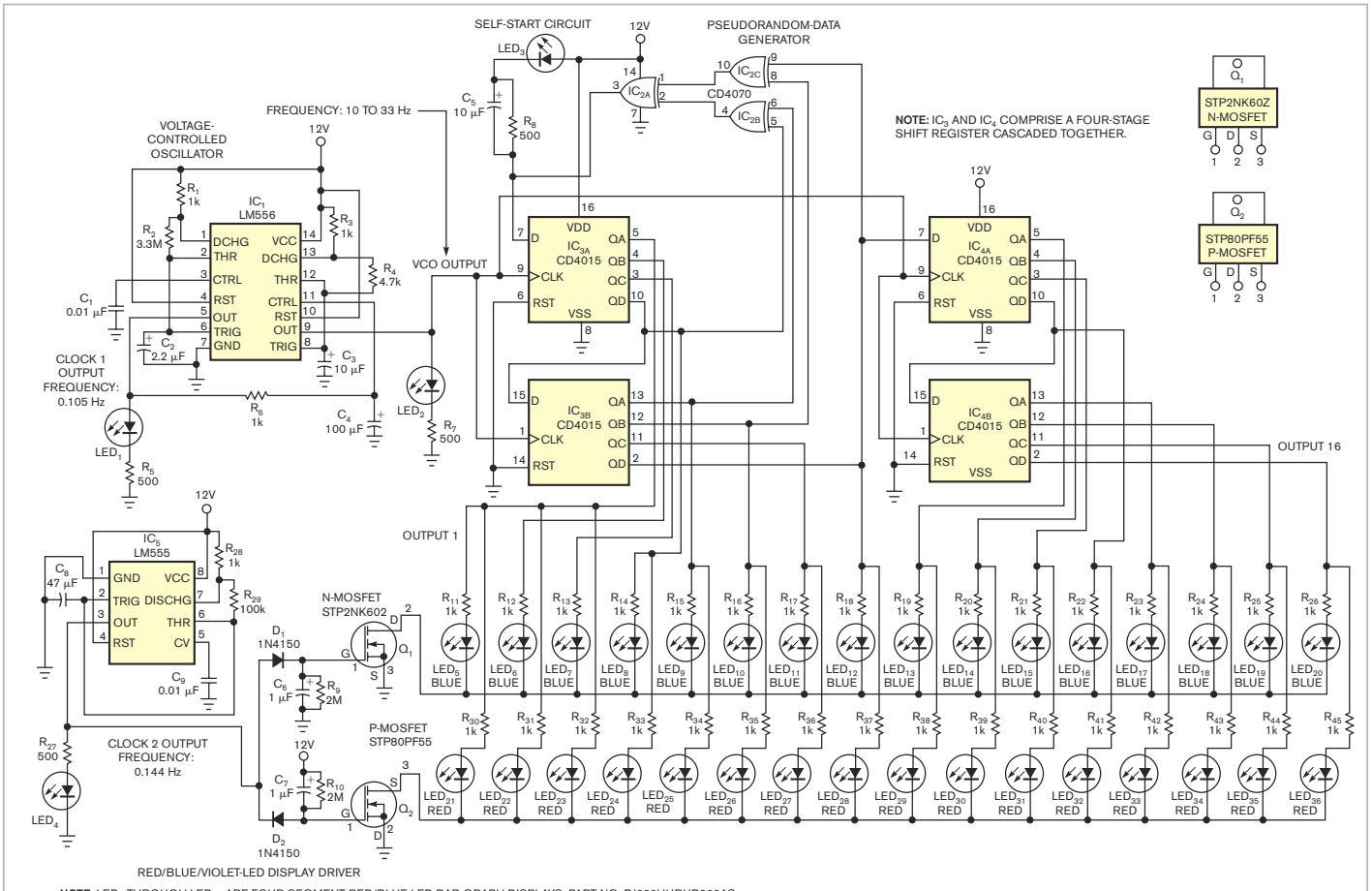


Figure 1 Two 555 timers create the clock pulses that drive blue and red LEDs.

tion of the VCO from 10 to 33 Hz.

LED_3, C_5, and R_8 act as a self-start circuit. Without it, you would need to add a pushbutton switch to toggle the data input of IC_{3A} from low to high during start-up. IC_2, a CD4070 quad exclusive-OR gate, acts as a pseudorandom-data generator. This circuit gives the illusion that bits of data span the bar graph.

IC_3 and IC_4 are CD4015 four-stage shift registers cascaded together. The data bits span the bar-graph displays in sequence from Output 1 to Output 16. IC_5, an LM555 timer, produces Clock 2's frequency of approximately 0.144 Hz. The inverse of this frequency toggles high to low approximately every 7 seconds, feeding the gates of N-MOSFET Q_1 and P-MOSFET Q_2, which act as the red/blue/violet LED-display driver. Clock 2 toggles high, enabling Q_1 and giving the blue LEDs a source to ground.

When Clock 2 toggles low, Q_2 turns on, giving the red LEDs a path to ground. C_6 and C_7, together with R_9 and R_{10}, respectively, act as a slow discharge circuit on the gates of the MOSFETs, keeping them on for approximately 2 seconds longer than Clock 2's pulse. The delay lets both the blue and the red LEDs be on at the same time for approximately 2 seconds and produces the color violet. This circuit uses N- and P-channel MOSFETs from ST-Microelectronics (www.st.com), but any general-purpose MOSFET should work. Just make sure that each one can handle at least 0.5A.

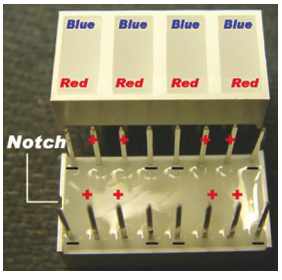


Figure 2 The bar graphs have both red and blue LEDs; turning on both yields violet.

The four-segment red/blue-LED bar-graph displays are unique. Each bar-graph display comprises one red and one blue LED in the same bar (**Figure 2**). Each LED has its own anode and cathode connections, thereby keeping this circuit simple without the need to add extra transistor drivers for each LED. You'd have to add them if their anodes, cathodes, or both were connected. This circuit requires four bar-graph displays. If you install any of the LED bar graphs backward, you will see the second color displayed, so that, if you were expecting red, you would get blue, and vice versa. EDN

Control stepper motors in both directions

Vladimir Rentyuk, Modul-98 Ltd, Zaporozhye, Ukraine

Stepper motors need bidirectional control in automatic machines or robotic applications. The circuit in **Figure 1** lets you control bipolar stepper motors and run them in both rotations. You can use the circuit in automatic devices and as an evaluation circuit for testing stepper motors. The circuit comprises clock oscillators IC_{3A} and IC_{3B}; a bidirectional, two-phase translator using an SN74HC74D dual flip-flop, IC_2, with a directional selector, IC_{3C} and IC_{3D}; and a push-pull L293DD channel-driver, IC_1. The circuit needs one power source, which depends on the stepper-motor specification. You can use a step-down voltage regulator to provide 5V dc. In many applications, an L7805A voltage regulator is suitable. Switch S_2 turns the motor on, and switch S_1 controls the motor's direction. Both signals can come from a sensor or a circuit with an open-collector output.

A circuit surrounding transistor Q_1 starts the motor. A forced starting is necessary because generators that employ two CMOS or TTL inverters are sometimes unstable after powering and can oscillate at a frequency of approximately 18 MHz. Thus, you need a delay after applying power to

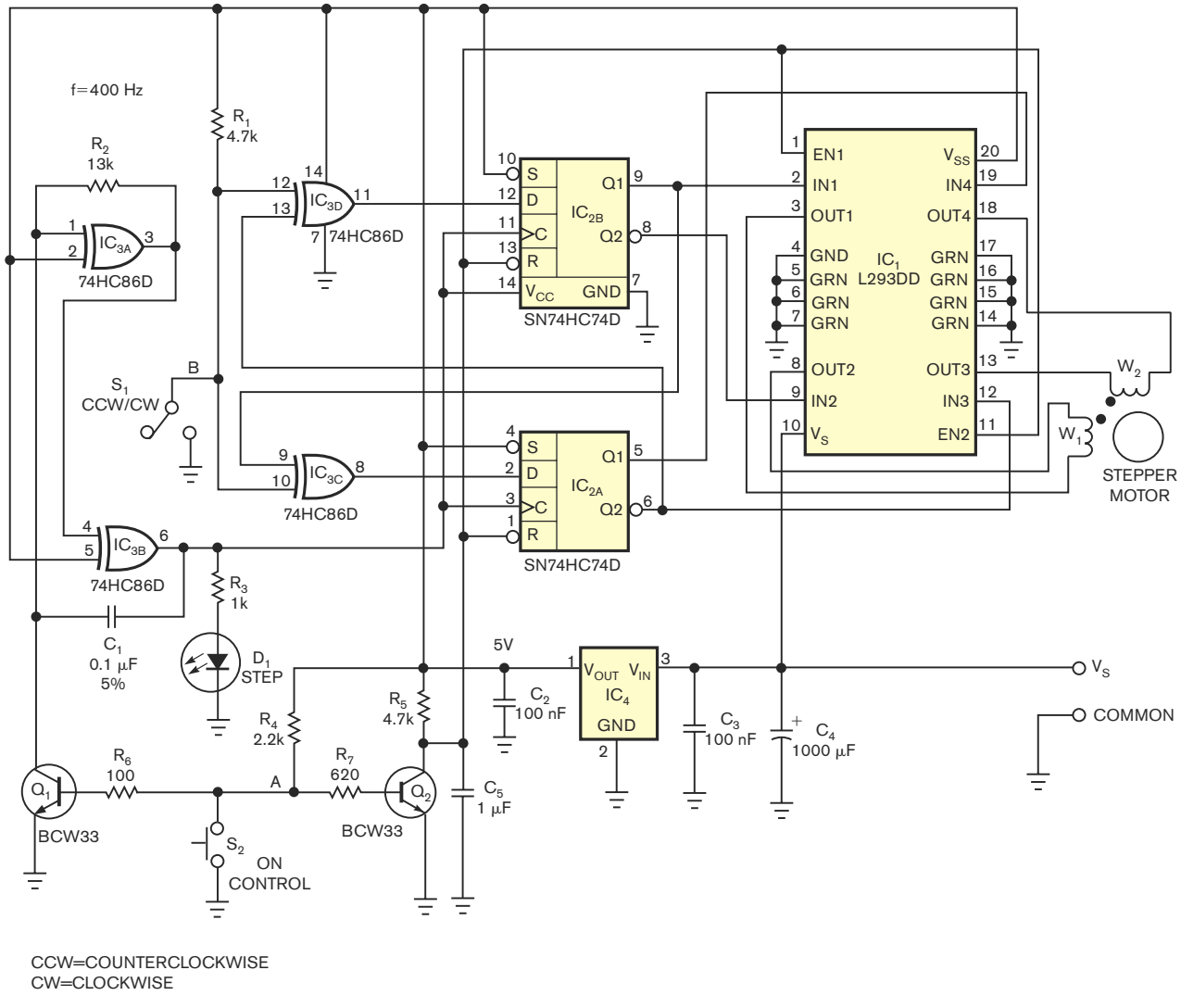
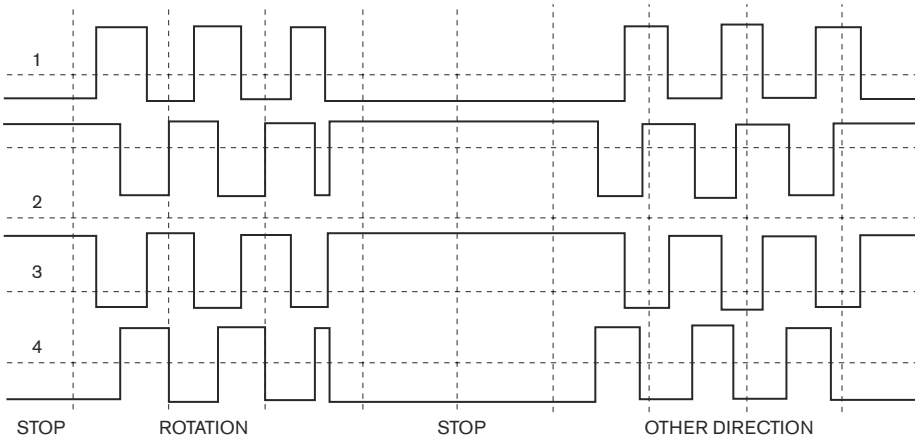


Figure 1 This circuit provides the necessary signals to drive a stepper motor. Switches turn the motor on and off and change its direction.

the circuit before sending the "on" command. The delay must be at least 100 µsec, but a delay of a few milliseconds is best. Capacitor C_5 eliminates the negative influence of bounce from S_2's contacts. The rotation of a rotor of the stepper motor begins when S_2 presents a low level to Point A. C_5 is unnecessary if a low-level signal from a circuit with an open collector comes to Point A—but not mechanical switches or buttons. Switch S_1 can be any suitable signal, such as that from a safety stop switch with a timer, trigger, or any open-collector output that connects to Point B. LED D_1 is a step indicator in "on" mode.



NOTES:
TRACE 1: OUTPUT Q1 OF IC_{2B} (IN1 OF IC_1).
TRACE 2: OUTPUT Q2 OF IC_{2A} (IN3 OF IC_1).
TRACE 3: OUTPUT Q2 OF IC_{2B} (IN2 OF IC_1).
TRACE 4: OUTPUT Q1 OF IC_{2A} (IN4 OF IC_1).

Figure 2 The motor stops when the outputs of IC_{2A}'s Q1 and IC_{2B}'s Q1 stay low. EN1 and EN2 are low, too.

The speed of rotation of a stepper motor depends on its specification from a step angle of the stepper motor and the frequency of the clock oscillator. **Figure 2** shows a timing diagram of the reversal mode of the circuit. EDN

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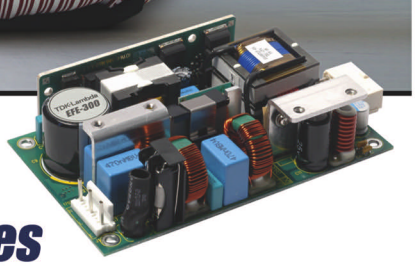

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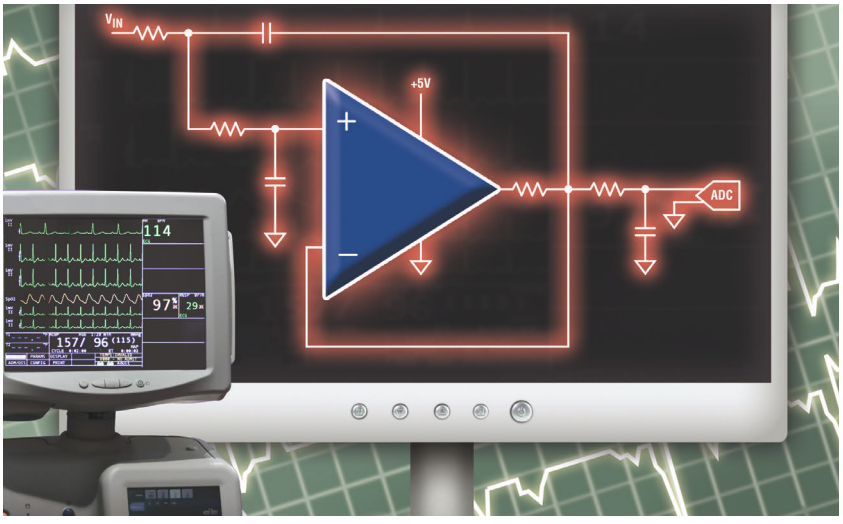

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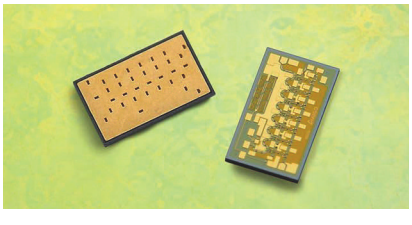
Maxim Integrated Products, www.maxim-ic.com

Traveling-wave amplifier aims at high-speed digital communications

The AMMC-5025 dc to 80-GHz traveling-wave amplifier suits high-speed digital-communications applications operating in the 30-kHz to 80-GHz frequency band, such as test-and-measurement equipment, radar-warning receivers, wideband communications and surveillance systems, and point-to-point radios. The device provides 8-dB small-signal gain, ±0.7-dB gain flatness, and a 10-dB input and output return loss. A gain-slope-control feature and adjustable gain control enable a dynamic range of more than 25 dB. Features include a 50Ω match on input and output and 300V HBM ESD protection. Available in a 1.6×1-mm die, the AMMC-5025 costs $150 (1000).



Avago Technologies, www.avagotech.com

Single-ended-to-differential amplifier drives 16-bit ADCs

The 33-MHz, low-noise, rail-to-rail, single-ended-to-differential LT6350 amplifier settles to 16 bits in 350 nsec. The device integrates two op amps and matched resistors, creating a differential output from a single-ended, high-impedance input. The input-and-output ADC driver has a 1.9-nV/$\sqrt{Hz}$ input-referred noise density, resulting in a total 8.2-nV/$\sqrt{Hz}$ output-referred noise. Operating on a 2.7 to 12V total supply, the device consumes 4.8 mA of supply current. The amplifier suits 0 to 70, −40 to +85, and −40 to +125°C commercial-, industrial-, and extended-temperature ranges, respectively. Available in lead MSOP-8 and 3×3-mm DFN packages, the LT6350 ADC costs $2.59 (1000).

Linear Technology, www.linear.com

Class D audio amplifier has a PDM digital interface

The PDM (pulse-density-modulation) SSM2517 digital-input Class D audio amplifier suits use in handsets, portable media players, and laptop computers. The amplifier combines an audio DAC, a power amplifier, and a PDM digital interface. Digitally transmitting the audio to the amplifier minimizes the effect of the GSM interference or other sources of electrically coupled noise. Claiming 90% power efficiency, the closed-loop-modulator design enables a reliable rejection of power-supply ripple. Available in a 1.5×1.5-mm, nine-ball WLCSP package, the SSM2517 audio amplifier costs 63 cents (1000).

Analog Devices, www.analog.com

COMPUTERS AND PERIPHERALS

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NEC Display Solutions of America, www.necdisplay.com

Multiflash readers use high-speed SATA interface

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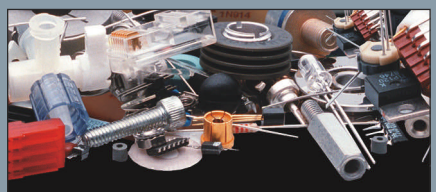

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Seeing red over dead LEDs

DANIEL VASCONCELLOS

Years ago, I was the manufacturing engineer for a large electronics manufacturer. My employer had contracted a front-panel design to a major supplier for a new military-product contract. The design comprised a standard keypad with dome switches and three surface-mount LEDs as indicators of power-on, power-standby, and system-down conditions. A different color and location under the overlay window indicated each of these modes. The board received 5V of power from an external source, and some current-limiting resistors on the panel biased the LEDs. We received 10 prototypes in five weeks, and I evaluated them for form, fit, and function and found no problems. I signed off on qualifying the manufacturer, and the purchasing department ordered the requisite number of parts for the first month of the production run.

When the front panels arrived, we installed them without an intermediate test, thinking they should be just like the prototypes. Almost immediately, the production technicians complained that the contract manufacturer had installed some LEDs backward, and they would not light. Some were the wrong color, and some correctly installed LEDs were dead. Failures were random and did not affect every panel. Because we were up against a production schedule on a military contract with significant penalties, I chose to repair the panels in-house and just report the failures to the panel manufacturer.

An engineer at the manufacturer assured me that his people knew the difference between the anode and the cathode on an LED but admitted that he couldn't explain the problems we were seeing during testing. I suggested that he test the panels before shipping them. He instead proposed that we switch from manual placement and reflow to an automated process. At least the panels would be consistently good—or bad.

Sure enough, the next month's panels were consistent: All the red and green LEDs were installed backward, so they wouldn't light. I applauded the manufacturing engineer for consistency but again suggested that he test each panel. I returned some of the extra panels, and he called a few days later to tell me that he had reworked the problems with the panels.

When we received the final month's panels, the red and green LEDs were again backward. The manufacturer had correctly installed the blue LEDs, though. I immediately sent some panels back to the manufacturer's engineer. He assured me that he had witnessed engineers testing some of the panels, that they had all passed, and that the problem had to be at our end.

A few days went by, and we were able to complete the contract by reworking the panels ourselves again. Just as we were about to test the last few assemblies, the manufacturing engineer called to tell me that he and his production manager had witnessed all three LEDs lighting up during the test, and they found no problems. I then asked the test engineer to place the positive test lead of a digital multimeter on what should be the anode on the panel trace leading to the red LED and place the other lead on what should be the cathode. I told him to switch the meter to ac. He read 18V ac. Sure enough, those LEDs were going to light up on the fixture whether they were backward or not!

You might wonder why a test engineer would use an ac source to test the polarity on an LED. I have been an engineer for 20 years, and I have seen a lot of ugly things, so I didn't even ask. EDN

Pat Sheets is a manufacturing engineer at Aeroflex Test Solutions (Wichita, KS).

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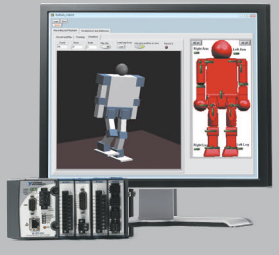

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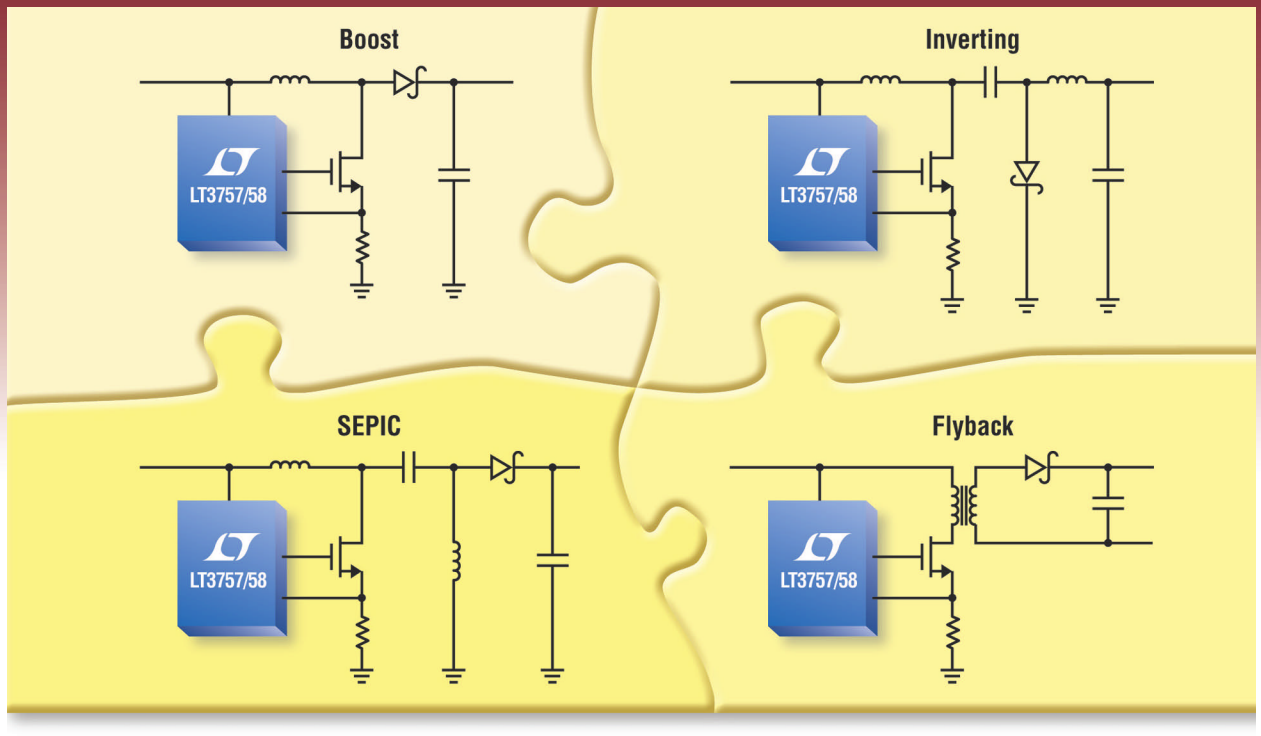

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LT3755	4.5V to 40V	Boost, Flyback, SEPIC, Inverting, LED Driver	Controller*	3mm x 3mm QFN-16, MSOP-16E
LT3756	6.0V to 100V		Controller*	3mm x 3mm QFN-16, MSOP-16E
LT3757	2.9V to 40V	Boost, Flyback, SEPIC, Inverting	Controller*	3mm x 3mm DFN-10, MSOP-10E
LT3758	5.5V to 100V		Controller*	3mm x 3mm DFN-10, MSOP-10E
LT3956	6.0V to 80V	Boost, Flyback, SEPIC, Inverting, LED Driver	Monolithic, 3A	5mm x 6mm QFN
LT3957	3.0V to 40V	Boost, Flyback, SEPIC, Inverting	Monolithic, 4.5A	5mm x 6mm QFN
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